NATIONAL OPEN UNIVERSITY OF NIGERIA

COURSE CODE:-CIT 236

COURSE TITLE:-
ANALOGUE AND DIGITAL ELECTRONICS

COURSE GUIDE

CIT 236
ANALOGUE AND DIGITAL ELECTRONICS

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Introduction

Analogue and Digital Electronics is a 3-credit unit course of eleven units. It is an introductory course which seeks to introduce the students to the basic concepts of analogue and digital electronics. It provides an introduction to the different types of transistors, the biasing arrangements and the configuration of the transistor amplifiers. It also covers the basic principles of feedback and operational amplifiers. The DC power supply is also covered together with voltage regulators heatsinks and finally the text provides an introduction to digital electronics by treating Boolean algebra, logic gates and karnaugh maps. The course is divided into four modules.

Module 1 introduces the transistor, its biasing and the different amplifier configuration of the transistor amplifier. The block lays the foundation for the understanding of the electronics circuit analysis and design.

Module 2 covers the principles of feed back and the operational amplifier. The different types of feedback topolofies and the application

of the different feedback types together with the application of the operational amplifier are covered in this module.

Module 3 describes the DC power supply systems and covers the analysis of the different component parts and it also provides an insight into the design of voltage regulators and heatsinks.

Module 4 has its focus on Digital electronics. It treats the principles of Boolean algebra, logic gates and karnaugh maps. The different types of logic gates and the laws governing Boolean algebra are treated in this module.

The aim of this course is to equip you with the basic skills of analysis and design of electronic circuits as well lay a foundation for the understanding of analogue and digital electronics.

This Course Guide gives you a brief overview of the course content, course duration, and course materials.

What You Will Learn in this Course

The main purpose of this course is to provide the foundational information and theories necessary for the understanding of electronics and the necessary tool for the analysis and design of analogue and digital electronics this, we intend to achieve through the following:

Course Aims

2. Introduces you to the concepts associated with transistors and the transistor amplifiers.
3. Introduces you to the concepts associated with feedback circuits, operational amplifiers and DC power supply design;
4. Expose you to basic principle of Digital electronics, Boolean algebra and logic gates.

Course Objectives

Certain objectives have been set out to ensure that the course achieves its aims. Apart from the course objectives, every unit of this course has set objectives. In the course of the study, you will need to confirm, at the end of each unit, if you have met the objectives set at the beginning of each unit. By the end of this course you should be able to:

i. Identify different types of transistors and the configurations;
ii. Describe the design of feed back circuits and the different feedback topologies.

iii. Explain the principles behind the design of operational amplifier based circuit.
iv. Understand the analysis and design of DC power supplies and voltage regulators.
v. Describe the principles and operation of Boolean algebra and the logic gates.

Working through the Course

In order to have a thorough understanding of the course units, you will need to read and understand the contents, practise what you have learnt by studying the network of your organization or proposing one if there is none in existence and be committed to learning and implementing your knowledge.

This course is designed to cover approximately sixteen weeks, and it will require your devoted attention. You should do the exercises in the Tutor-Marked Assignments and submit to your tutors.

Course Materials

These include:

1. Course Guide
2. Study Units
3. Recommended Texts
4. A file for your assignments and for records to monitor your progress.

Study Units

There are seventeen study units in this course:

Module 1

Unit 1 Biploar Junction Transistors
Unit 2 Small signal Amplifiers
Unit 3 Field Effect Transistors

Module 2

Unit 1 Introduction to feedback
Unit 2 Operational Amplifiers

Module 3

Unit 1 DC power supplies
Unit 2 Voltage regulators
Unit 3 Heat sinks

Module 4

Unit 1 Boolean Algebra
Unit 2 Logic gates
Unit 3 Karnaugh Maps

Make use of the course materials, do the exercises to enhance your learning.

Textbooks and References

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

Ron Macini; Op Amps for Everyone. Design Reference, Texas Instruments.

Mendelson, Elliott, (1970). *Schaum's Outline of Theory and Problems of Boolean Algebra.* McGraw- Hill.

Electronics for Dummies by Gordon McComb and Earl Boysen. (2005). Wiley Publishing.

Assignment File

These are of two types: the self-assessment exercises and the Tutor-Marked Assignments. The self-assessment exercises will enable you monitor your performance by yourself, while the Tutor-Marked Assignment is a supervised assignment. The assignments take a certain percentage of your total score in this course. The Tutor-Marked Assignments will be assessed by your tutor within a specified period. The examination at the end of this course will aim at determining the level of mastery of the subject matter. This course includes seventeen Tutor-Marked Assignments and each must be done and submitted accordingly. Your best scores however, will be recorded for you. Be sure to send these assignments to your tutor before the deadline to avoid loss of marks.

Presentation Schedule

The Presentation Schedule included in your course materials gives you the important dates for the completion of tutor marked assignments and

attending tutorials. Remember, you are required to submit all your assignments by the due date. You should guard against lagging behind in your work.

Assessment

There are two aspects to the assessment of the course. First are the tutor marked assignments; second, is a written examination.

In tackling the assignments, you are expected to apply information and knowledge acquired during this course. The assignments must be submitted to your tutor for formal assessment in accordance with the deadlines stated in the Assignment File. The work you submit to your tutor for assessment will count for 30% of your total course mark.

At the end of the course, you will need to sit for a final three-hour examination. This will also count for 70% of your total course mark.

Tutor-Marked Assignment

There are seventeen tutor marked assignments in this course. You need to submit all the assignments. The total marks for the best four (4) assignments will be 30% of your total course mark.

Assignment questions for the units in this course are contained in the Assignment File. You should be able to complete your assignments from the information and materials contained in your set textbooks, reading and study units. However, you may wish to use other references to broaden your viewpoint and provide a deeper understanding of the subject.

When you have completed each assignment, send it together with form to your tutor. Make sure that each assignment reaches your tutor on or before the deadline given. If, however, you cannot complete your work on time, contact your tutor before the assignment is done to discuss the possibility of an extension.

Examination and Grading

The final examination for the course will carry 70% of the total marks available for this course. The examination will cover every aspect of the course, so you are advised to revise all your corrected assignments before the examination.

This course endows you with the status of a teacher and that of a learner. This means that you teach yourself and that you learn, as your learning capabilities would allow. It also means that you are in a better position to determine and to ascertain the what, the how, and the when of your course learning. No teacher imposes any method of leaning on you.

The course units are similarly designed with the introduction following the table of contents, then a set of objectives and then the concepts and so on.

The objectives guide you as you go through the units to ascertain your knowledge of the required terms and expressions.

Course Marking Scheme

This table shows how the actual course marking is broken down.

Assessment	**Marks**
Assignment 1- 4	Four assignments, best three marks of the four count at 30% of course marks
Final Examination	70% of overall course marks
Total	100% of course marks

Table 1: Course Marking Scheme

Course Overview

Unit	**Title of Work**	**Weeks Activity**	**Assessment (End of Unit)**
	Course Guide	Week 1	
	Module 1		
1	Bipolar Junction Transistors	Week 1-2	Assignment 1
2	Small Signal Amplifiers	Week 3	Assignment 2
3	Field Effect Transistors	Week 4	Assignment 3
	Module 2		
1	Introduction to Feedback	Week 5-6	Assignment 4

2	Operational Amplifiers	Week 7-8	Assignment 5
	Module 3		
1	Dc power Supplies	Week 9-10	
2	Voltage Regulators	Week 11	
3	Heat Sink Design	Week 12	Assignment 6
	Module 4		
1	Boolean Algebra	Week 13	Assignment 7
2	Logic Gates	Week 14	Assignment 8
3	Karnaugh Maps	Week 15	
	Revision	**Week 16**	
	Examination	**Week 17**	
	Total	**17 weeks**	

How to Get the Best from this Course

In distance learning the study units replace the university lecturer. This is one of the great advantages of distance learning; you can read and work through specially designed study materials at your own pace, and at a time and place that suit you best. Think of it as reading the lecture instead of listening to a lecturer. In the same way that a lecturer might set you some reading to do, the study units tell you when to read your set books or other material. Just as a lecturer might give you an in-class exercise, your study units provide exercises for you to do at appropriate points.

Each of the study units follows a common format. The first item is an introduction to the subject matter of the unit and how a particular unit is integrated with the other units and the course as a whole. Next is a set of learning objectives. These objectives enable you know what you should be able to do by the time you have completed the unit. You should use these objectives to guide your study. When you have finished the units you must go back and check whether you have achieved the objectives. If you make a habit of doing this you will significantly improve your chances of passing the course.

Remember that your tutor's job is to assist you. When you need help, don't hesitate to call and ask your tutor to provide it.

1 Read this Course Guide thoroughly.

2 Organize a study schedule. Refer to the 'Course Overview' for more details. Note the time you are expected to spend on each unit and how the assignments relate to the units. Whatever method you chose to use, you should decide on it and write in your own dates for working on each unit.

3 Once you have created your own study schedule, do everything you can to stick to it. The major reason that students fail is that they lag behind in their course work.

4 Turn to Unit 1 and read the introduction and the objectives for the unit.

5 Assemble the study materials. Information about what you need for a unit is given in the 'Overview' at the beginning of each unit. You will almost always need both the study unit you are working on and one of your set of books on your desk at the same time.

6 Work through the unit. The content of the unit itself has been arranged to provide a sequence for you to follow. As you work through the unit you will be instructed to read sections from your set books or other articles. Use the unit to guide your reading

7 Review the objectives for each study unit to confirm that you have achieved them. If you feel unsure about any of the objectives, review the study material or consult your tutor.

8 When you are confident that you have achieved a unit's objectives, you can then start on the next unit. Proceed unit by unit through the course and try to pace your study so that you keep yourself on schedule.

9 When you have submitted an assignment to your tutor for marking, do not wait for its return before starting on the next unit. Keep to your schedule. When the assignment is returned, pay particular attention to your tutor's comments, both on the tutor-marked assignment form and also written on the assignment. Consult your tutor as soon as possible if you have any questions or problems.

10 After completing the last unit, review the course and prepare yourself for the final examination. Check that you have achieved the unit objectives (listed at the beginning of each unit) and the course objectives (listed in this Course Guide).

Facilitators/Tutors and Tutorials

There are 12 hours of tutorials provided in support of this course. You will be notified of the dates, times and location of these tutorials, together with the name and phone number of your tutor, as soon as you are allocated a tutorial group.

Your tutor will mark and comment on your assignments, keep a close watch on your progress and on any difficulties you might encounter and provide assistance to you during the course. You must mail or submit your tutor-marked assignments to your tutor well before the due date (at least two working days are required). They will be marked by your tutor and returned to you as soon as possible.

Do not hesitate to contact your tutor by telephone, or e-mail if you need help. The following might be circumstances in which you would find help necessary. Contact your tutor if:

- you do not understand any part of the study units or the assigned readings,
- you have difficulty with the self-tests or exercises,
- you have a question or problem with an assignment, with your tutor's comments on an assignment or with the grading of an assignment.

You should try your best to attend the tutorials. This is the only chance to have face to face contact with your tutor and to ask questions which are answered instantly. You can raise any problem encountered in the course of your study. To gain the maximum benefit from course tutorials, prepare a question list before attending them. You will learn a lot from participating in discussions actively.

Summary

Analogue and Digital Electronics introduces you to the basic concepts of analogue and digital electronics. It provides an introduction to the different types of transistors, the biasing arrangements and the configuration of the transistor amplifiers. It also covers the basic principles of feedback and operational amplifiers. The DC power supply is also covered together with voltage regulators heatsinks and finally the text provides an introduction to digital electronics by treating Boolean algebra, logic gates and karnaugh maps. The content of the course material was planned and written to ensure that you acquire the proper knowledge and skills for the appropriate situations. Real-life situations have been created to enable you identify with and create some of your own. The essence is to get you to acquire the necessary knowledge and

competence, and by equipping you with the necessary tools, we hope to have achieved that.

I wish you success with the course and hope that you will find it both interesting and useful.

Course Code	CIT 236
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MODULE 1

Unit 1 Bipolar Junction Transistors
Unit 2 Small Signal Amplifiers
Unit 3 Field Effect Transistors

UNIT 1 BIPOLAR JUNCTION TRANSISTORS

CONTENTS

1.0 INTRODUCTION

A transistor is a three-terminal semiconductor device that can be used for amplification and switching**.** Amplification consists of magnifying a signal by transferring energy to it from an external source; whereas a transistor switch is a device for controlling a relatively large current between or voltage across two terminals by means of a small control current or voltage applied at a third terminal. There are two major families of transistors are *bipolar junction transistors*, or *BJTs*; and *field-effect transistors*, or *FETs. A*s will be shown, the BJT acts essentially as a current-controlled device, while the FET behaves as a voltage-controlled device.

2.0 OBJECTIVES

At the end of this unit, students should be able to:

- be able to IDENTIFY basic transistor amplifier topologies
- be able to ANALYZE basic amplifier topologies for gains and resistances
- be able to DISCUSS the relative properties of various amplifier topologies
- be able to DESIGN basic amplifiers to meet or exceed stated specifications.

3.0 MAIN CONTENT

3.1 The Bipolar Junction Transistor (BJT)

The *pn* junction forms the basis of a large number of semiconductor devices. A BJT is formed by joining three sections of semiconductor material, each with a different doping concentration. The three sections can be either a thin *n*region sandwiched between *p*+ and *p* layers, or a *p* region between *n* and *n*+ layers, where the superscript "plus" indicates more heavily doped material. The resulting BJTs are called *pnp* and *npn* transistors, respectively:

The figure 1.1 below shows the block diagrams and circuit symbols of both the npn ad the pnp transistors.

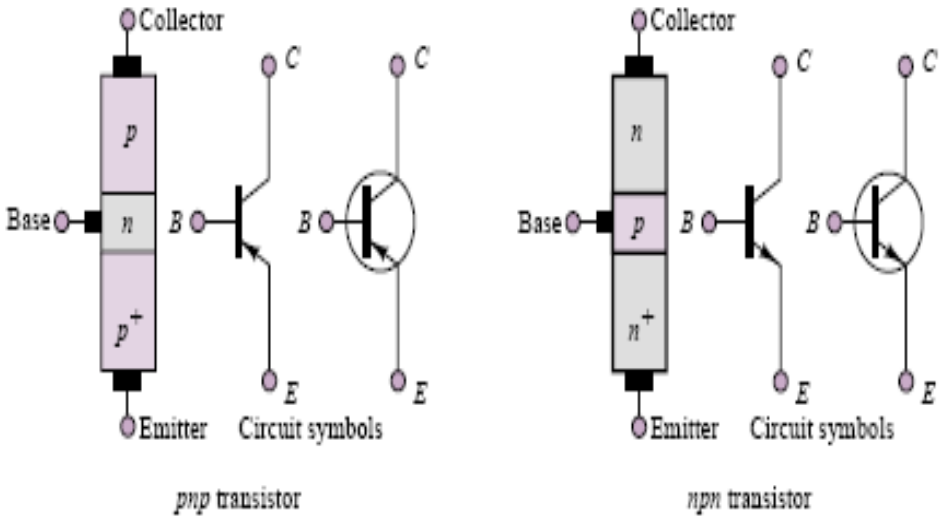


Figure 1.1 transistor symbols

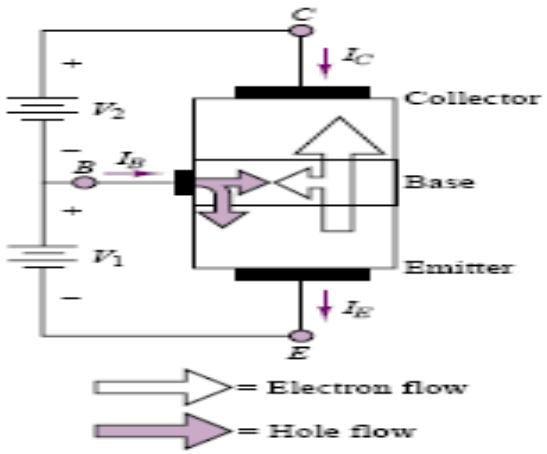


Figure 1.2 electron flows in transistors

The operation of the *npn* BJT can be explained by considering the transistor as consisting of two back-to-back *pn* junctions. The **base-emitter (*BE*) junction** acts very much like a diode when it is forward-

biased; thus, the corresponding flow of hole and electron currents from base to emitter when the collector is open and the *BE* junction is forward-biased, is shown in figure 1.2.Note that the electron current has been shown larger than the hole current, because of the heavier doping of the *n* side of the junction. Some of the electron-hole pairs in the base will recombine; the remaining charge carriers will give rise to a net flow of current from base to emitter. It is also important to observe that the base is much narrower than the emitter section of the transistor.

The flow of electrons in the transistor is represented by the equation below.

$I_E = I_B + I_C$ ……..1

Since the transistor is biased in the active region a small base current controls the much larger collector current.

Where $I_C = \beta I_B$……..2

where β is a current amplification factor dependent on the physical properties of the transistor. Typical values of β range from 20 to 200. The operation of a *pnp* transistor is completely similar to that of the *npn* device, with the roles of the charge carriers (and therefore the signs of the currents) reversed.

$I_E = I_B + \beta I_B$ …….3

$I_E = (1+\beta) I_B$ ……...…….4

from the equation (4) above

$I_B = \frac{I_E}{(1+\beta)}$ ……..……5

$I_C = \left(\frac{\beta}{1+\beta}\right) I_E$ ……..……..……..……6

Equation 6 can be written as $I_C = \alpha I_E$

Thus $\alpha = \left(\frac{\beta}{1+\beta}\right)$ where α = common base current gain.

3.2 Bipolar Junction Transistor Configurations

Transistors can be configured in three different modes with one pair of terminals for the input and another pair for the output. These configurations are:

1. Common emitter
2. Common collector
3. Common base.

- **Common Emitter**

In the common emitter configuration, the input terminal is the base while the output terminal is the collector and the emitter is common to both the input and the output as shown in figure 1.3 below.

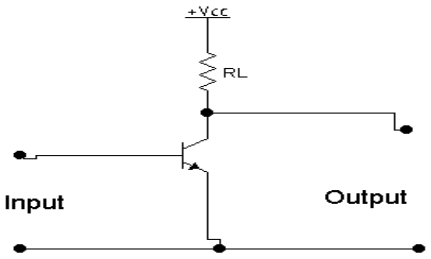


Figure 1.3 Common Emitter configurations

The current gain for this configuration is given by $\frac{output\_current}{input\_current} = \frac{I_C}{I_B}$

- **Common Collector**

In the common collector configuration, the input terminal is the base while the output terminal is the emitter and the collector is common to both the input and the output as shown in figure 3.4 below.

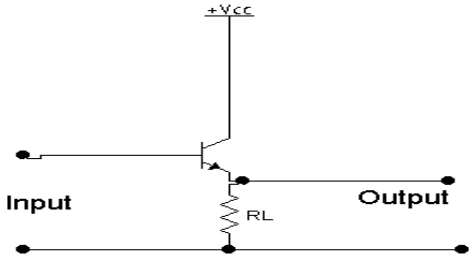


Figure 1.4 Common collector configurations

The current gain for this configuration is given by $\frac{I_E}{I_B}$

- **Common Base**

In the common base configuration, the input terminal is the emitter while the output terminal is the collector and the base is common to both the input and the output as shown in figure 1.5 below

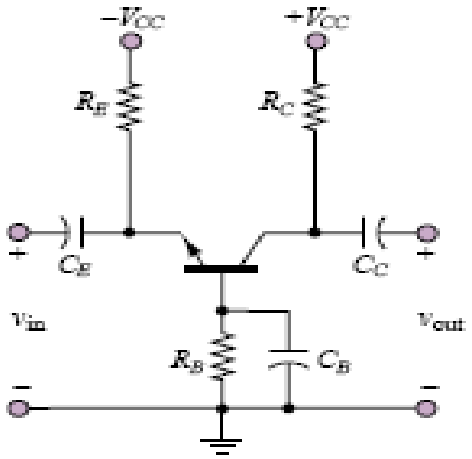


Figure 1.5 common base configuration

The current gain for this configuration is given by $\frac{I_C}{I_E}$

The gain for the CB configuration is always less than 1, so the CB configuration is not used for current amplification .The CC and CE configurations both have a high gain but the input impedance of the CE configuration is higher than that of the CC. This makes the CE configuration the preferred choice for amplifiers in circuit design.

3.3 Loads Lines

The load line is a line drawn based on the DC operating characteristics of the circuit. It enables the visualization of the transistor characteristics. It is determined by using the DC equations of the circuit. The Ic (max) and Vce (max) are used to determine the end points of the line, these points are then joined together and superimposed on the transistor characteristics.

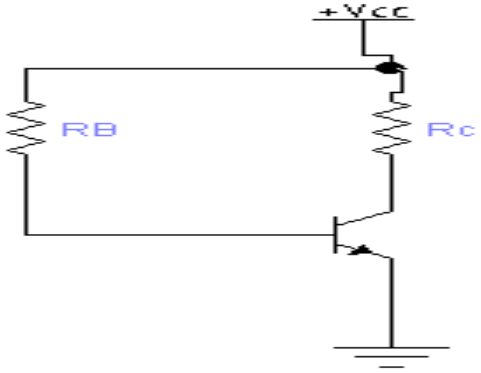


Figure 1.6 Amplifier circuit

From the circuit 1.6, the analysis is done below

From the output equation

$V_{cc} = I_C R_C + V_{CE}$

The load line is determined by identifying the two endpoints of the line. The are determined by assuming $V_{CE} = 0$ and finding Ic, and the V subscribe is determined by assuming Ic= 0.

From the output equation, with Ic = 0,

$Vcc = V_{CE}$

With $V_{CE} = 0$

Vcc = IcRc

$$Ic(max) = \frac{Vcc}{Rc}$$

The load line is sketched in the figure 1.7 below

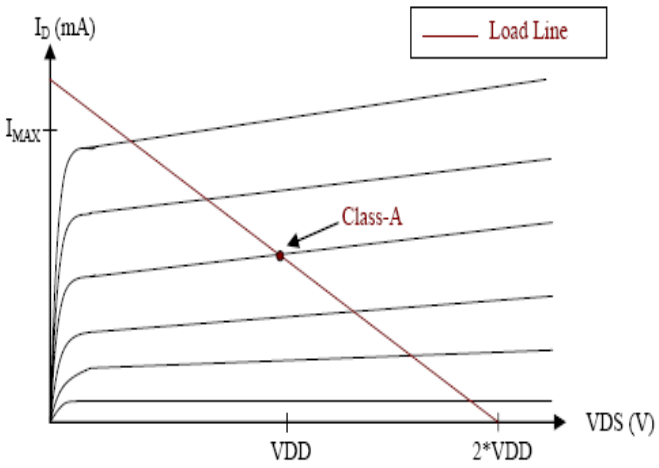


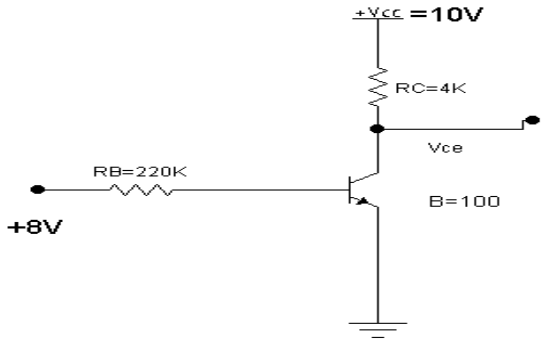
Figure 1.7 load line

The curves are generated at different base currents. The Q point (operating Point) is the intersection of the Ic and the Vce on the load line for any particular base current.

From the graphs, as Ic rises from 0, the mode of operation of the transistor changes from cutoff to active and when the Ic gets to the maximum, the transistor gets to the saturation region of operation.

Example 1

Given the circuit below, determine the load line.



From the output equation

$V_{cc} = I_C R_C + V_{CE}$

With Vce = 0

$$\text{Ic(max)} = \frac{10}{4K} = 2.5mA$$

With Ic = 0

Vce = 10V

3.4 Bipolar Junction Transistor Biasing

The transistor can serve either as a switch or an amplifier. The mode of operation of each transistor is determined by the bias condition in which it operates.

Biasing can be defined as the setting up of the DC voltages and current in an electronic circuit.

From the output characteristics, the transistor has 3 regions of operation.

(i) Saturation region
(ii) Active region
(iii) Cutoff region

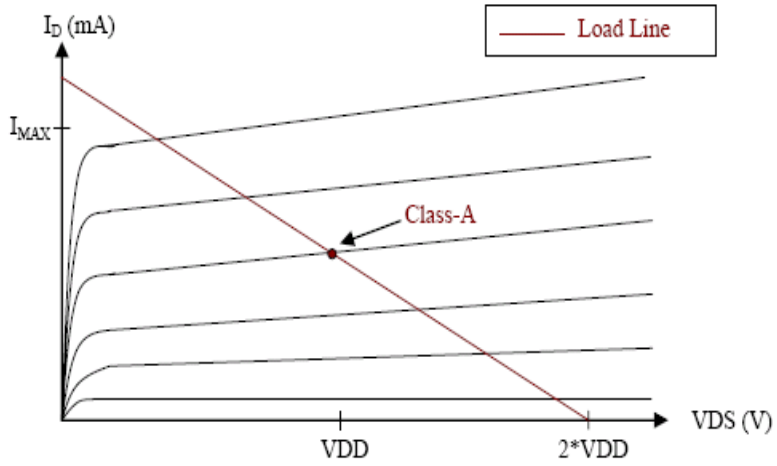


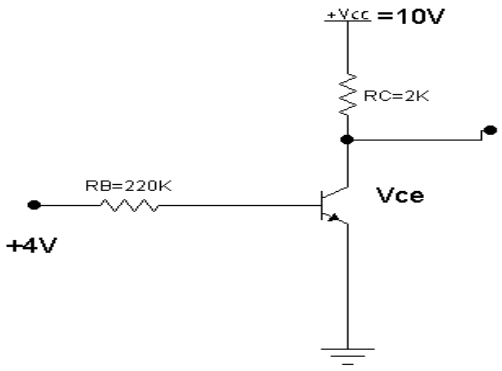
Figure 1.8 Q-point

The Q point or dc operating point is that point on the load line where the I_{cq} and V_{ceq} intercept on the load line. The transistor when operating as a switch is biased in the saturation or cutoff region but for the transistor to be used as an amplifier it is biased in the active region. With transistor in the forward active region the voltage across the B-E junction is V subscribe (on) is 0.7V for silicon transistors and 0.4V for germanium transistors.

The determination of the q point is through the process of biasing.

Example 2

Calculate the base, collector and emitter currents for the circuit shown below.β =200



From the output equation

$Vcc = IcRc + V_{CE}$

From the input equation

$V_{BB} = I_B R_B + V_{BE}$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{4 - 0.7}{220K} = 15\mu A$$

$Ic = \beta I_B = (200)(15\mu A) = 3mA$

$I_E = (1+\beta).\ I_B = (200+1)\ (15\mu A) = 3.02mA$

$V_{CE} = Vcc - IcRc = 10 - (3mA)(2K) = 4V$

3.5 Types Common Emitter Biasing

There are different types of bias circuit with each having its advantages and disadvantages.

1. Base Bias

This is the simplest type and is also known as fixed bias. The quiescent base current is established by a single base resistor as shown in figure 1.9 below.

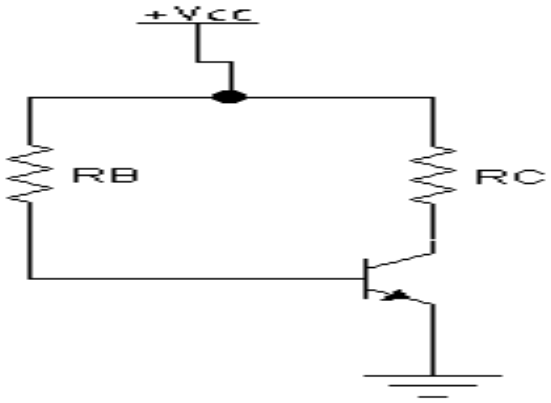


Figure 1.9 base bias

Biasing of this circuit will involve the selection of appropriate values for the base resistance and collector resistance.

Analysis

Input equation

$V_{cc} = I_B R_B + V_{BE}$ _____(1)

$I_B R_B = V_{CC} - V_{BE}$ _____(2)

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$$ _____(3)

$$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}}$$ _____(4)

This equation yields the Quiescent base current I_{BQ}

From the circuit, the output equation is derived below

$V_{cc} = I_C R_C + V_{CE}$ _____(5)

$I_{CQ} R_C = V_{CC} - V_{CE}$ _____(6)

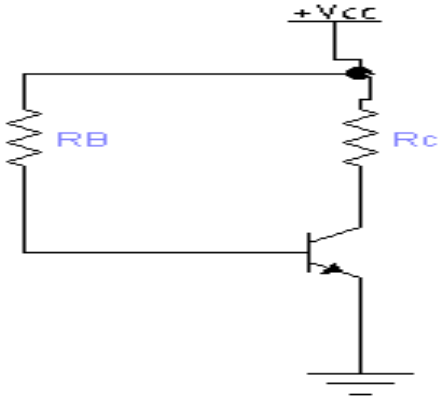
$$I_{CQ} = \frac{V_{CC} - V_{CE}}{R_C}$$ _____(7)

$$R_C = \frac{V_{CC} - V_{CE}}{I_{CQ}}$$ _____(8)

Example 3

Given the circuit below, design the amplifier for the following specifications:

$V_{CC} = 12V$, $\beta = 100$, $V_{be} = 0.7$, $I_{cq} = 1_m A$ $V_{ceq} = 6V$



Solution

From the input equation,

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B R_B = V_{CC} - V_{BE} = 12 - 0.7$$
$$I_B R_B = II.3V$$

From the output equation

$$V_{cc} = I_c R_c + V_{ce}$$
$$I_c R_c = V_{cc} - V_{ce} = 12 - 6$$
$$Ic = \frac{12 - 6}{1mA} = 6K\Omega$$
$$\frac{Icq}{I_{BQ}} = \beta$$
$$\therefore I_{BQ} = \frac{Icq}{\beta} = \frac{1mA}{100} = 10\mu A$$

The base resistance is determined from the input equation to be

$$I_{BQ} R_B = V_{CC} - V_{be}(on)$$
$$R_B = \frac{12 - 0.7}{10\mu A} = 1.13M\Omega$$

The load line is determined to be

$Vcc = IcRc + Vce$

$Ic = 0,$

$Vce = Vcc = 12V$

$Vce = 0$

$$Ic = \frac{Vcc}{Rc} = \frac{12}{6K} = 2mA$$

From the various formulas used above, the Icq is dependent to a large extent on the β. The beta (β) varies with temperature so any circuit built with too much dependence on β will be very unstable.

- **Base Bias with Collector Feedback**

The base is connected to the collector as shown in the circuit in figure 1.10 below

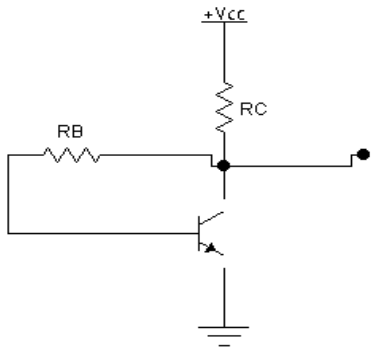


Figure 1.10 Base bias with collector feedback

Output equation

$V_{CC} = (I_C + I_B)R_C + V_{CE}$ ……..1

The collector current and the base currents flow through the collector resistor

But $I_C >> I_B$

$$\text{IC(sat)} = \frac{Vcc}{Rc}$$

Since there is no emitter resistor the out put equation becomes

$V_{CC} = (I_C + I_B)R_C + V_C$

$V_C = Vcc - (I_C + I_B)R_C$

Since Vc also forms part of the input equation, the input equation becomes

$$V_C = I_B R_B + V_{BE}$$

$$Vcc - (I_C + I_B)R_C = I_B R_B + V_{BE}$$

Since $I_C >> I_B$

$$Vcc - I_C R_C = I_B R_B + V_{BE}$$

But $I_B = \frac{Ic}{\beta}$

$$\frac{IcR_B}{\beta} + V_{BE} = Vcc - I_C R_C$$

The collector current can be derived from the expression below.

$$Ic = \frac{Vcc - V_{BE}}{\frac{R_B}{\beta} + Rc} \approx I_E$$

From the expression for collector current, the effect of the transistor gain on the collector current is reduced leading to better system stability

- **Base Bias with Collector and Emitter Feedback**

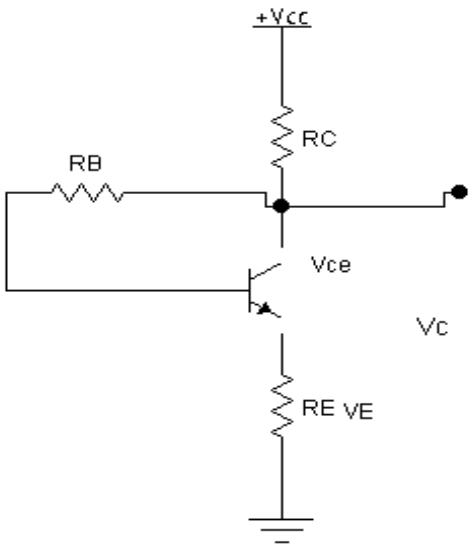


Figure 1.11 Base Bias with collector and emitter feedback

From the output equation

$$V_{CC} = (I_C + I_B)R_C + V_{CE} + I_E R_E$$

$I_C >> I_B$ and $I_C = I_E$

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E = V_{CE} + I_C(R_C + R_E)$$

$$I_C = \frac{V_{CC} - V_{CE}}{(R_E + R_C)}$$

At saturation (V_{CE} =0)

$$I_C = \frac{V_{CC}}{(R_E + R_C)}$$

The actual value of Ic is derived using the input equation since in most cases the V_{CE} is unknown

From the input equation

$$V_{CC} = I_C R_C + V_{BE} + I_B R_B + I_E R_E$$

Since $I_C = I_E$

$$V_{CC} = I_C R_C + V_{BE} + I_B R_B + I_C R_E$$

$$V_{CC} - V_{BE} = I_C(R_C + R_E) + I_B R_B$$

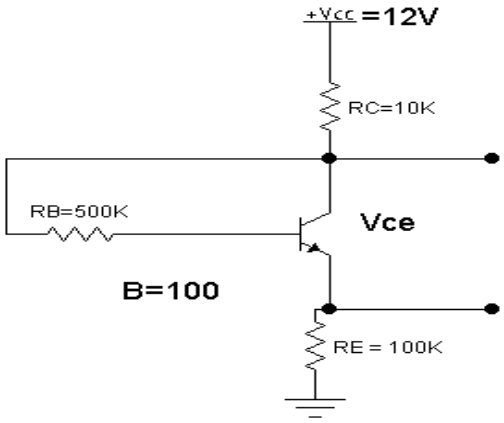
But $I_B = \frac{I_C}{\beta}$

$$V_{CC} - V_{BE} = I_C(R_C + R_E) + \frac{R_B}{\beta}$$

$$I_C = \frac{V_{CC} - V_{BE}}{(R_E + R_C + \frac{R_B}{\beta})}$$

Example 4

Determine the Ic(sat),V_{CE} and Vc. In the circuit below. Neglect V_{BE}



From the output equation

$$V_{CC} = (I_C + I_B)R_C + V_{CE} + I_E R_E$$

$I_C >> I_B$ and $I_C = I_E$

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E = V_{CE} + I_C(R_C + R_E)$$

$$I_C = \frac{V_{CC} - V_{CE}}{(R_E + R_C)}$$

At saturation (V_{CE} =0)

$$I_C(sat) = \frac{12}{(100K + 10K)} = 0.11mA$$

$V_C = V_{CE} + V_E$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$V_E = I_E R_E$

To determine I_C we use the input equation

$$V_{CC} = I_C R_C + V_{BE} + I_B R_B + I_E R_E$$

Since $I_C = I_E$

$$V_{CC} = I_C R_C + V_{BE} + I_B R_B + I_C R_E$$

$$V_{CC} - V_{BE} = I_C(R_C + R_E) + I_B R_B$$

But $I_B = \frac{I_C}{\beta}$

$$V_{CC} - V_{BE} = I_C(R_C + R_E) + \frac{R_B}{\beta}$$

$$I_C = \frac{V_{CC} - V_{BE}}{(R_E + R_C + \frac{R_B}{\beta})}$$

$$I_C = \frac{12}{(10k + 100k + \frac{500k}{100})} = \frac{12}{115k} = 0.1\text{mA}$$

Substituting the value of I_C in the equation for V_{CE} we have

$$V_{CE} = V_{CC} - I_C(R_C + R_E) = 12 - 0.1mA(110K) = 1V$$

$V_C = V_{CE} + V_E = 1 + I_C R_E = 1 + 0.1\text{mA}(100\text{K}) = 11\text{V}$

- **Voltage Divider Bias**

From the circuit diagram in figure 1.12, the voltage divider bias is analyzed below as follows.

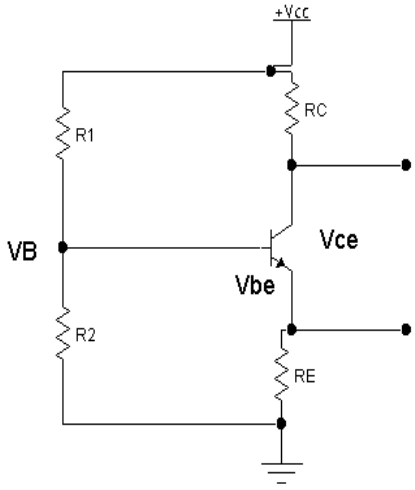


Figure 1.12 Voltage divider bias

From the potential (voltage) divider equation

$$VB = \frac{Vcc * R2}{R1 + R2}$$

VB = Vbe + VE

VE = VB – Vbe but VB >>Vbe

$$IE = \frac{VE}{RE} = \frac{VB - Vbe}{RE} = \frac{VB}{RE}$$

From the output equation

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_C = V_{CE} + V_E$$

$$V_{CE} = V_{CC} - I_C(R_E + R_C)$$

With $V_{CE} = 0$ in the output equation, Ic is determined as

$$I_C(sat) = \frac{Vcc}{R_E + R_C}$$

The base voltage is set by the resistors R1 and R2 thus the effect of the transistor forward gain is reduced .The D.C bias is independent of β.

4.0 CONCLUSION

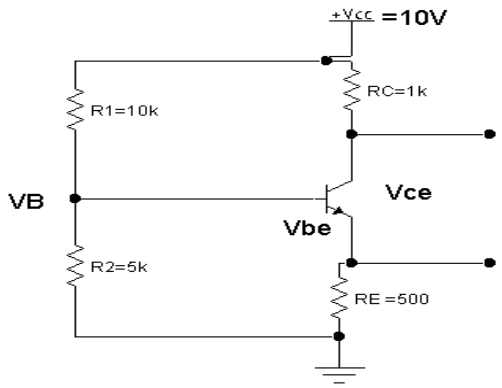
In this unit you have been introduced to the transistor amplifier and the different types of biasing arrangements and transistor configurations.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of transistors and transistor amplifier design.

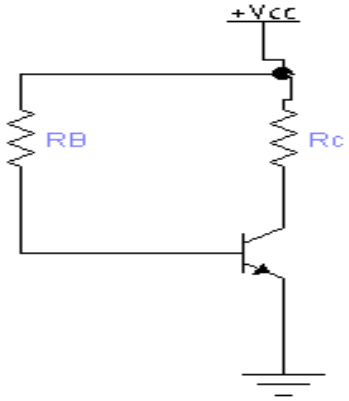
6.0 TUTOR-MARKED ASSIGNMENT

1. Determine the V_{CE} and I_C in the circuit diagram shown below. Vbe = 0.7



2. Given the circuit below, design the amplifier for the following specifications:

$V_{CC} = 12V$, $\beta = 100$, $V_{be} = 0.7$, $I_{cq} = 1_mA$ $V_{ceq} = 6V$



7.0 REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

UNIT 2 SMALL SIGNAL AMPLIFIERS

CONTENTS

1.0 INTRODUCTION

Electronic amplifying devices such as BJT and FET have three terminals (E,B,C and S,G,D).In a basic amplifying circuit, one of the terminals is made common while the other two serve as input and output ports. **Small-signal models** for the BJT take advantage of the relative linearity of the base and collector curves in the vicinity of an operating point. These linear circuit models work very effectively, providing that the transistor voltages and currents remain within some region around the operating point. This condition is usually satisfied in small-signal amplifiers used to magnify low-level signals (e.g., sensor signals). For the purpose of our discussion, we use the **hybrid-parameter (*h*-parameter) small-signal model** of the BJT, to be discussed presently. Note that a small-signal model assumes that the DC bias point (Q-point) of the transistor has been established. The following convention will be used: each voltage and current is assumed to be the superposition of a DC component (the quiescent voltage or current) and a small-signal AC component. The former is denoted by an uppercase letter and the latter by an uppercase letter preceded by the symbol Δ. Thus,

$iB = IBQ + \Delta IB$

$iC = ICQ + \Delta IC$

$vCE = VCEQ + \Delta VCE$

2.0 OBJECTIVES

At the end of this unit, student should be able to:

- be able to IDENTIFY the transistor hybrid parameters
- be able to ANALYZE amplifier topologies for gains and impedances
- be able to DISCUSS the relative properties of various amplifier configurations
- be able to DESIGN basic amplifiers to meet or exceed stated specifications.

3.0 MAIN CONTENT

3.1 Transistor Hybrid parameters

The Hybrid parameters are specifications used in the analysis of transistor amplifiers there are four *h* parameters and these are:

- The parameter *hie* which is approximately equal to the ratio Δ *VBE/* Δ*IB*. Physically, this parameter represents the forward resistance of the *BE* junction.

- The parameter *hre* which is representative of the fact that the *IB-VBE* curve is slightly dependent on the actual value of the collector-emitter voltage, *VCE*. However, this effect is virtually negligible in any applications of interest to us. Thus, we shall assume that *hre* $\approx$ 0. A typical value of *hre* for *VCE* $\geq$ 1 V is around 10^{-2}.

- The parameter *hf e* is the current ratio Δ *IC* /Δ*IB*. This parameter represents the current gain of the transistor and is approximately equivalent to the parameter β introduced earlier. For the purpose of our discussion, β and *hf e* will be interchangeable, although they are not exactly identical.

- The parameter *hoe* may be calculated as *hoe* = Δ*IC/* Δ *VCE From* the collector characteristic curves. This parameter is a physical indication of the fact that the *IC-VCE* curves in the linear active region are not exactly flat; *hoe* represents the upward slope of these curves and therefore has units of conductance (S). Typical values of *hoe* are around 10^{-5} S. this parameter is often assumed to be negligible.

$$h_{ie} = \left.\frac{\partial v_{BE}}{\partial i_B}\right|_{I_{BQ}} \quad (\Omega)$$

$$h_{oe} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{V_{CEQ}} \quad (\mathrm{S})$$

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{I_{BQ}} \quad \left(\frac{\mathrm{A}}{\mathrm{A}}\right)$$

$$h_{re} = \left.\frac{\partial v_{BE}}{\partial v_{CE}}\right|_{V_{CEQ}} \quad \left(\frac{\mathrm{V}}{\mathrm{V}}\right)$$

3.2 Analysis of a Single Stage Transistor Amplifier Small Signal Operation

In order to fully analyze a transistor amplifier, the analysis is broken into AC and DC analysis. In the DC analysis all capacitors are regarded as open circuits, while for the AC analysis, the capacitors are regarded as short circuits and the DC source is replaced by a ground.

The purpose of the analysis is to determine the different specifications of the circuit. These specifications include the input impedance, output impedance and the circuit gain.

Example 1

Given the circuit below, determine the *Q* point voltage and current values and AC open-loop voltage gain of the amplifier of Figure 2.1; the amplifier employs a 2N5088 *npn* transistor. β=350

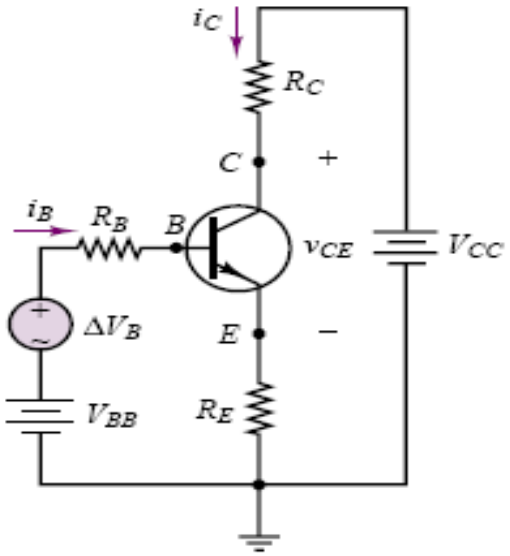


Figure 2.1

- **Analysis**

Q-point calculation

We first write the collector circuit equation by applying KVL:

$VCC = VCE + RCIC + REIE = VCE + RCIC + RE(IB + IC)$

$\approx VCE + (RC + RE)IC$

where the emitter current has been approximately set equal to the collector current since the current gain is large and $IC >> IB$.

Next, we write the base circuit equation, also via KVL:

$VBB = RBIB + VBE + REIE = (RB + (\beta + 1)RE)IB + Vbe$

The above equation can be solved numerically (with $hfe = \beta$) to obtain:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{6 - 0.6}{100 \times 10^3 + 351 \times 100} = 40\mu A$$

Then,

$IC = \beta IB = 350 \text{ X } 40 \text{ x } 10^{-6} = 14 \text{ mA}$

And

$VCE = VCC - (RC + RE)IC = 12 - 600 \text{ x } 40 \text{ x } 10^{-3} = 3.6 \text{ V}$

Thus, the Q point for the amplifier is:

$IBQ = 40\ \mu\text{A}$, $ICQ = 14$ mA and $VCEQ = 3.6$ V

Confirming that the transistor is indeed in the active region.

From previous discussion, it has been verified that the common emitter configuration is the best for signal amplification. We shall be looking at the single stage common emitter amplifier.

Any amplifier circuit has the following parts:

1) The Bias Circuit
2) The Load Circuit
3) The Coupling Circuit

The bias circuit has been discussed so we focus on the other component parts.

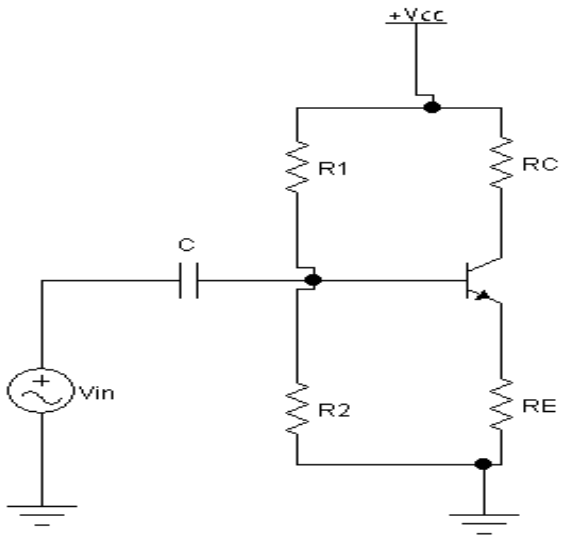


Fig 2.2: CE amplifier circuit

From the diagram above, the following are the responsibility of the different components.

C = Coupling capacitor. it prevents dc signals in the source from upsetting the amplifier's Q point values.

R_1 and R_2 = potential divider bias resistors

R_C = load/collector resistor

R_E = Emitter resistor

Given a common emitter amplifier circuit, to analyze such a circuit we need to consider its DC and AC characteristics.

Example 2

Given the circuit with the following parameters below, (βdc =150 and βac = 160)

Where βdc =DC gain and βac = AC gain. Determine the circuit specifications given the following component parameters. RE = 600Ω Rc = 1kΩ R1 = 22kΩ R2= 4.7kΩ

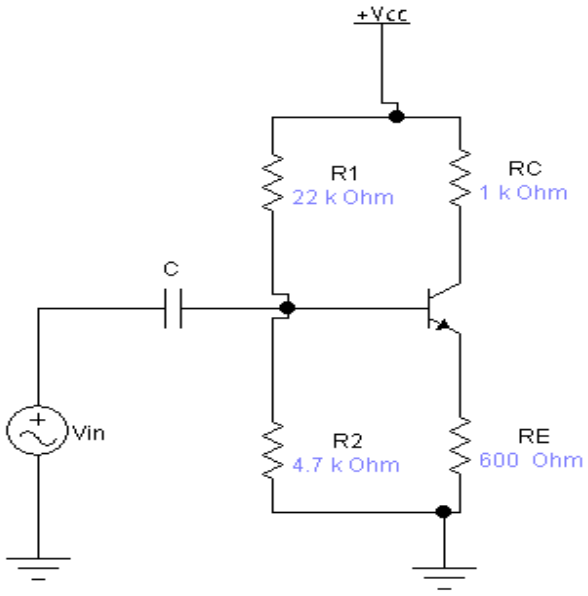


Fig 2.3: CE amplifier circuit

In order to understand the operation of the circuit given above, we will have to perform both the DC and AC analysis.

- **DC Analysis**

Before the DC analysis is performed, all coupling capacitors are regarded as open circuit. This will yield the following representation of the circuit above.

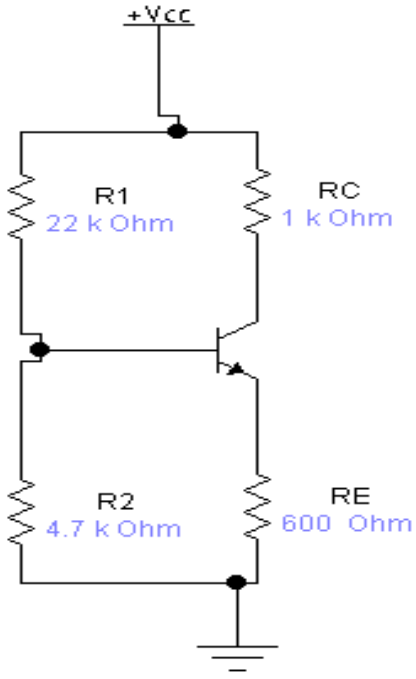


Fig 2.4:

From Ohms Law,

$$Rin = \frac{Vin}{Iin}$$

Vin =Vbe + $I_E R_E$. Vbe = 0.7 for silicon transistor which is the most widely used type. $I_E R_E >>$ Vbe

Vin = $I_E R_E$

$$Rin = \frac{I_E R_E}{Iin}$$

$Vin = IinRin = I_E R_E$ but IE ≈ Ic = βIb . The base current Ib is the input current and RIN is the resistance at the base so,

Iin = Ib and RIN = RB

$Vin = \beta IbR_E$ =IbRB

$RB = \frac{\beta IbR_E}{Ib}$ canceling Ib from both the numerator and denominator we have the DC input resistance RB to be, $RB = \beta R_E$

Inserting the values of the components,
The Dc input resistance of the circuit is give by

RIN = $RB = \beta dcR_E$ =150 x 600 = 90KΩ

Note: If RB is more than 10 times R2 then the voltage divider rules is used

$$VB = \left(\frac{R2}{R1 + R2}\right)Vcc = \left(\frac{4.7k}{22k + 4.7k}\right)x12 = 2.11V$$

VE =VB –Vbe =2.11 – 0.7=1.41V

$$IE = \frac{VE}{RE} = \frac{1.41}{600} = 2.4mA$$

Since Ic =IE

VC = Vcc- IcRC = 12 – 2.4 = 9.6V

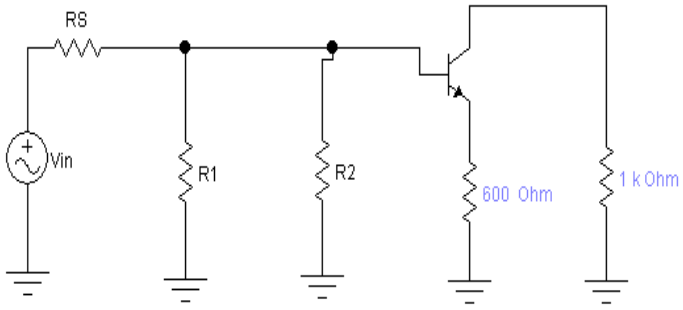
VCE = VC –VE = 9.6 – 1.41 = 8.19V

- **AC Analysis**

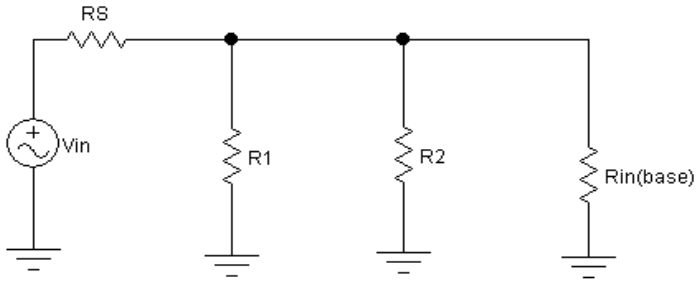
For the ac analysis the circuit is redrawn with the following assumptions.

1. All capacitors are short circuit

2. DC sources are replaced by ground



This circuit is further reduced to the circuit shown below



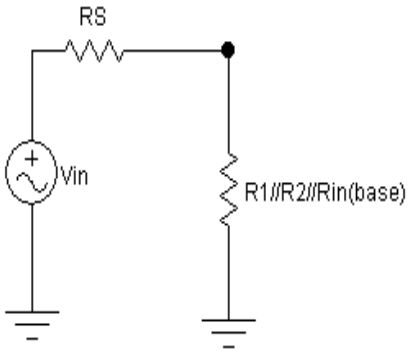
Rin (base) is the resistance at the base of the transistor and it is derived with the ac emitter resistance added in series to the RE.

Rin (base) = βac(re + RE)

The ac emitter resistance is given by $re = \frac{25mV}{IE}$

3.3 Input Impedance

The total input impedance of the circuit is the parallel combination of R1 ,R2 and Rin(base).Thus the circuit is reduced to the following



Input Impedance = R1//R2//Rin(base).

From the component values of the circuit assuming a source impedance of 300Ω, the input impedance is computed to be

Rin(base) = 160(re + 600)

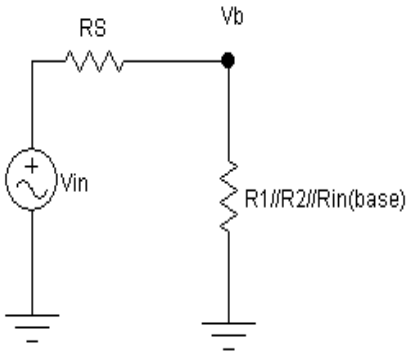
But $re = \frac{25mV}{IE} = \frac{25mV}{2.4mA} = 10.4\Omega$

IE is the DC emitter current computed to be 2.4mA.

Rin (base) = 160 (10.4 + 600)

Rin(base) =160(610.4) = 97664 Ω

The voltage at the base of the transistor (Vb) is determined below



If RS << Rin(input impedance) then Vb = Vin. If not then the voltage divider equation is used as shown below.

$$Vb = \left(\frac{Rin}{RS + Rin} \right) Vin$$

Compute the input impedance and the voltage at the base of the transistor

3.4 Output Impedance

The output resistance looking at the collector is approximately equal to R_C. In situations where a load is connected in parallel with the RC, the output resistance will be equal to the parallel combination of both the Rc and the load resistance. Thus a load (RL) connected to the output affects the gain.

RC1=RC//RL

3.5 Voltage Gain

The voltage gain is the ratio between the output voltage and the input voltage.

$$AV = \left(\frac{Output\_voltage}{Input\_voltage} \right)$$

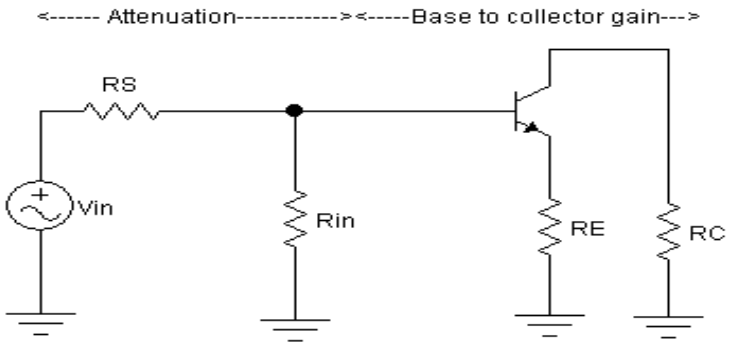
$$\frac{VC}{Vb} = \frac{IcRC}{IE(re + RE)}$$

$$\frac{IERC}{IE(re + RE)}$$

$$AV = \frac{RC}{(re + RE)}$$

This is the voltage gain from the base to the collector of the transistor.

The total circuit gain is made up of the attenuation due to the source resistance and the base to collector gain as shown below.



$$Vb = \left(\frac{Rin}{RS + Rin} \right) Vin$$

$$AV^{1} = \frac{RC}{(re + RE)}\left(\frac{Vb}{Vin}\right)$$

3.6 Effects of Emitter Bypass Capacitor on the CE Amplifier

When a capacitor is connected across the emitter resistor it bypasses the RE as the capacitor acts as a sort circuit for the AC signals. Thus the Ac voltage gain becomes

$AV = \frac{RC}{(re)}$ RE is neglected and the gain increases.

This increase in gain however leads to a reduction in gain stability because the re (ac emitter resistance varies with temperature)

4.0 CONCLUSION

In this unit you have been introduced to the small signal operation of the BJT amplifier and the transistor hybrid parameters.

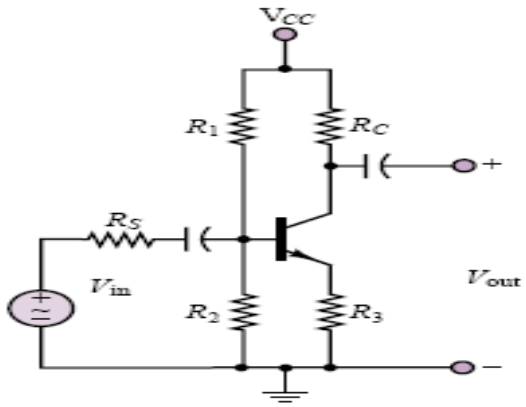
5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of transistors and small signal transistor amplifier design.

6.0 TUTOR-MARKED ASSIGNMENT

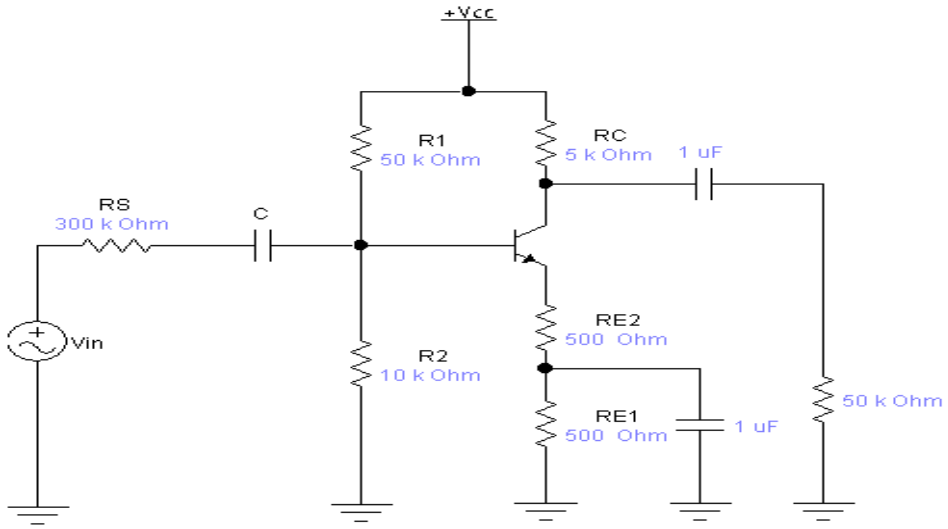
1. Determine the Q point of the amplifier shown below. *Vbe* = 0.7 V; β = 100; *VCC* = 15

V.*R*1 = 68 k_; *R*2 = 11.7 k_; *RC* = 200 _; *RE* = 200 _.



2. Given the amplifier circuit below determine the total output voltage (ac and dc).Vcc = 10V, βdc=150, β = 175 RS = 300Ω,R1 =50KΩ,R2 = 10KΩ, Rc = 5KΩ,

RE1=RE2 = 500Ω, Load =50KΩ



7.0 REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

UNIT 3 FIELD EFFECT TRANSISTORS

CONTENTS

1.0 INTRODUCTION

The concept upon which the field - effect transistor or FET is based is that the width of a conducting channel in a semiconductor may be varied by the external application of an electric field. Thus, FETs behave as *voltage-controlled resistors*. These devices can be grouped into three major categories. The first two categories are both types of metal-oxide-semiconductor field-effect transistors,or MOSFETs: enhancement-mode MOSFETs and depletion-mode MOSFETs. The third category consists of junction field-effect transistors, or JFETs. In addition, each of these devices can be fabricated either as an *n*-channel device or as a *p*-channel device, where the *n* or *p* designation indicates the nature of the doping in the semiconductor channel.

2.0 OBJECTIVES

At the end of this unit, students are expected be able to:

- be able to IDENTIFY field effect transistor symbols
- be able to ANALYZE basic FET amplifier topologies for gains and resistances
- be able to DISCUSS the relative properties of various FET configurations
- be able to DESIGN basic amplifiers to meet or exceed stated specifications.

3.0 MAIN CONTENT

3.1 Junction Field Effect Transistors

There are two general classes of FETs

(i) The Metal Oxide Semiconductor FET (MOSFET)
(ii) The Junction FET (JFET)

3.2 FET Configurations

The FET is similar to the BJT transistor in terms of the number of terminals and configuration. The FET has three terminals as shown below.

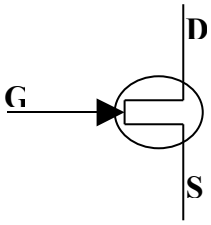
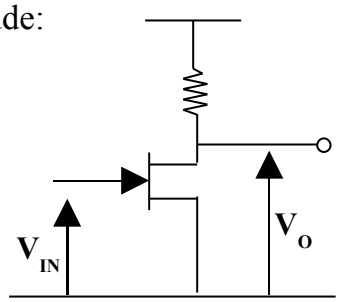


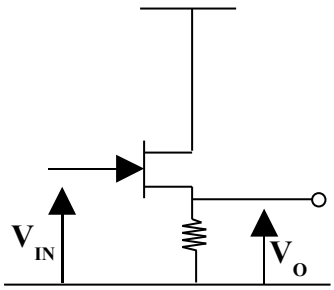
Fig 3.1 FET symbol

The configurations include:

(i) Common Source



(ii) Common Drain



(iii) Common Gate

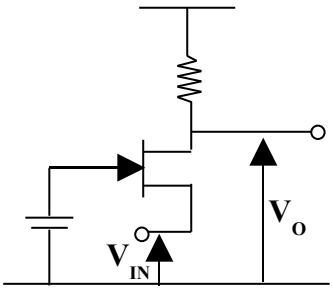


Fig 3.2 FET Configurations

The JFET is made up of a Semiconductor region known as the Channel with ohmic contacts at each end. The Channel material can either be N-type of P-type as shown below:

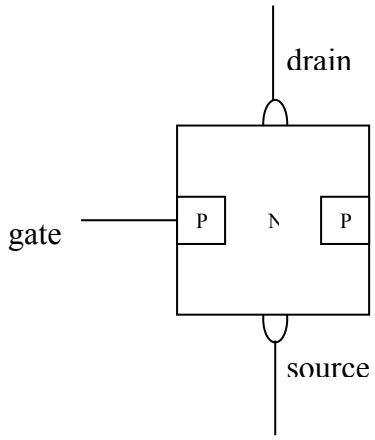


Fig 3.3 N channel JFET

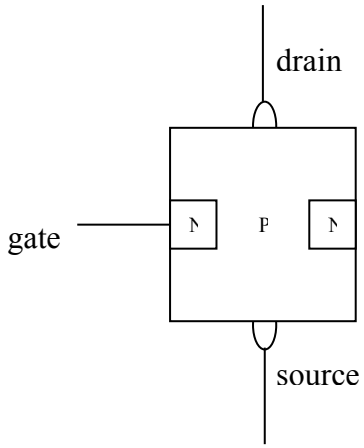


Fig 3.4 P channel JFET

The JFET is always operated with the Gate to Source voltage in Reverse Bias as shown below.

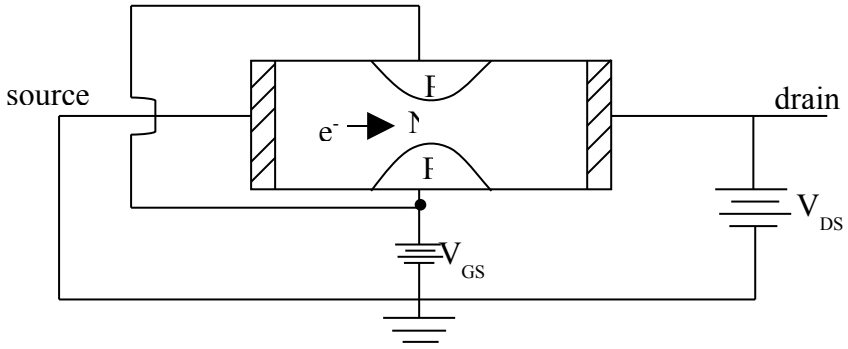


Fig 3.5 JFET Operation

In a P channel JFET, the P and N Junctions are reversed from those of the N Channel. In the P channel device, the Majority Carriers are holes (Positive Charges) and due to the low mobility of holes. The N-channel is often times preferred.

When V_{GS} is increased, more positive ions are injected into the P side and this narrows the depletion region there by widening the channel and increasing the current flow. When V_{GS} is decreased (made more negative), more positive ions are taken from the P side and the depletion region widens leading to a narrowing of the channel, reducing I_D flow. When V_{GS} becomes more negative to a point where ID=0, the conduction known as pinch-off arises.

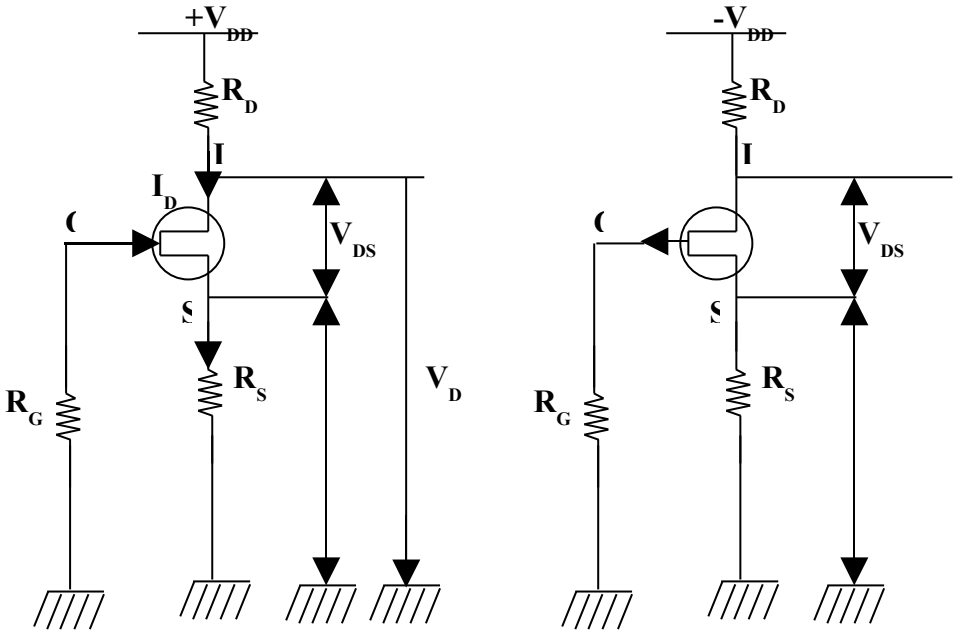
Drain current at Pinch-Off is essentially zero. The PN JFET is a normally-On device and its current flow is controlled by the gate and can only be switched off by applying a suitable voltage to the gate terminal

For the JFET,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

Where I_{DSS} = maximum value of I_D when $V_{GS} = 0$

$V_{GS(off)}$ = value of V_{GS} when FET will be off



Example 1

Given I_{DSS} = 12mA, $V_{GS\,(off)}$ = -5V, determine the value of I_D at V_{GS} = 0, -1, -4.

Solution:

For V_{GS} = 0

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = 12\text{mA}\left[1 - \frac{0}{-5V}\right]^2$$

$=12\text{mA}\,[1 + 0]^2 = 12\text{mA}$

For $V_{GS} = -1$

$$I_D = 12mA\left[1 - \frac{-1}{-5}\right]^2$$

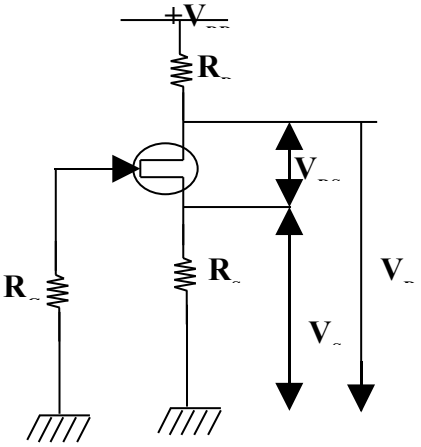
$$= 12mA\left[1 - \frac{1}{5}\right] = 7.68mA$$

For $V_{GS} = -4$

$$I_D = 12mA\left[1 - \frac{-4}{-5}\right]^2 = 12mA\left[1 - \frac{4}{5}\right]^2$$

$$= 0.48mA$$

For the N channel JFET,



$V_{DD} = I_D R_D + V_D$

$V_D = V_{DD} - I_D R_D$

$V_{GS} = V_G - V_S$

$V_{GS} = 0 - V_S$

$V_S = I_D R_S$

∴ For N channel, the $V_{GS} = -I_D R_S$

For P channel, the $V_{GS} = I_D R_S$

$V_{DD} = I_D R_D + V_{DS} + V_S$

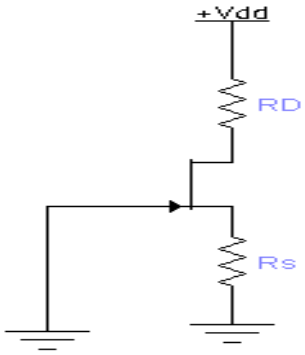
$V_S = I_D R_S$

$V_{DD} = I_D R_D + V_{DS} + I_D R_S$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

Example 2

Given the circuit below with the following transistor parameters of I_{DSS} = 5mA, $V_p = V_{GS} = -4V$, design the circuit such that $I_D = 2mA$, $V_{DS} = 6V$



Solution

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{Vp}\right)^2$$

$$2 = 5\left(1 - \frac{V_{GS}}{-4}\right)^2$$

$$\left(1 - \frac{V_{GS}}{-4}\right) = \sqrt{2/5}$$

Take the square root of both sides

$$\sqrt{\left(1 - \frac{V_{GS}}{-4}\right)^2} = \sqrt{0.4}$$

$$1 - \frac{V_{GS}}{-4} = 0.63$$

$$-\frac{V_{GS}}{-4} = 0.63 - 1 = -0.37$$

$$-V_{GS} = (-4)(-0.37) = 1.48$$

$$-V_{GS} = 1.48V$$

$$\therefore V_{GS} = -1.48V$$

From the diagram $I_DR_S = -V_{GS}$

$$\therefore I_D = \frac{-V_{GS}}{R_S}$$

$$\therefore R_S = \frac{-V_{GS}}{I_D} = \frac{1.48}{2mA} = 0.74K\Omega$$

From the output equation,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$V_{DS} = V_{DD} - I_D - I_D R_S$$

$$V_{DS} = 6V$$

$$\therefore R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} = \frac{10 - 6 - (2mA)(0.74K)}{2mA}$$

$$R_D = \frac{4 - 1.48}{2} = 1.26K\Omega$$

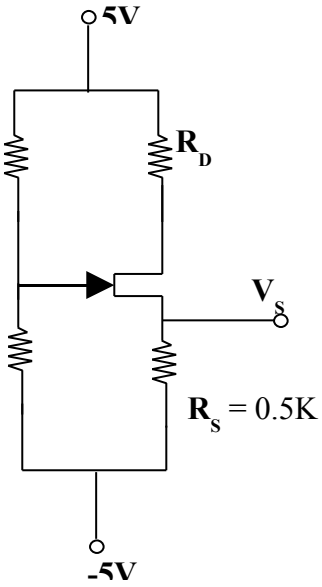
Example 3

Given the circuit below, the transistor parameters are I_{DSS} = 12mA, V_p = -3.5V, R_1+R_2 = 100K. Design the circuit such that I_D = 5mA, V_{DS} = 5V

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{Vp}\right)^2$$

$$5 = 12\left(1 - \frac{V_{GS}}{Vp}\right)^2$$

$$\frac{5}{12} = \left(1 - \frac{V_{GS}}{-3.5}\right)$$



Square root both sides

$$\sqrt{0.42} = \sqrt{\left(1 - \frac{V_{GS}}{-3.5}\right)}$$

$$0.65 = 1 - \frac{V_{GS}}{-3.5}$$

$$-\frac{V_{GS}}{-3.5} = -0.35$$

$$-V_{GS} = 1.24V$$

$$V_{GS} = -1.24V$$

From the circuit,

$$V_S = I_D R_S - 5 = (5)(0.5) - 5 = -2.5V$$

$$V_{GS} = V_G - V_S \therefore V_G = V_{GS} + V_S$$

$$V_{GS} = -1.24 + -2.5 = -1.24 - 2.5 = -3.74V$$

From potential divider

$$V_G = \frac{R2}{R1 + R2}(+V)$$

$$-3.74 = \frac{R2}{100}(10) - 5$$

$$\frac{R2}{100}(10) = -3.74 + 5$$

$$\frac{R2}{10} = 1.26K$$

$$R2 = 12.6K$$

$$R1 = 100K - 12.6K = 87.4K\Omega$$

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$\therefore R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} = \frac{10 - 5 - (5)(0.5)}{5}$$

$$R_D = \frac{10 - 5 - 2.5}{5} = 0.5K\Omega$$

4.0 CONCLUSION

In this unit you have been introduced to the Field effect transistor amplifier and the different types of biasing arrangements and FET configurations.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of transistors and transistor amplifier design.

6.0 TUTOR-MARKED ASSIGNMENT

Given I_{DSS} = 12mA, $V_{GS\,(off)}$ = -4V, determine the value of I_D at V_{GS} = 0, -1, -4.

7.0 REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design.* Second Edition Van Nostrand Reinhold Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

MODULE 2

Unit 1 Introduction to Feedback
Unit 2 Operational Amplifiers (OPAMPS)

UNIT 1 INTRODUCTION TO FEEDBACK

CONTENTS

1.0 INTRODUCTION

A feedback system is a system in which the input signal is modified by the system output before the internal processing by the system itself. The block diagram in a typical feedback system is shown in figure 4.1 below.

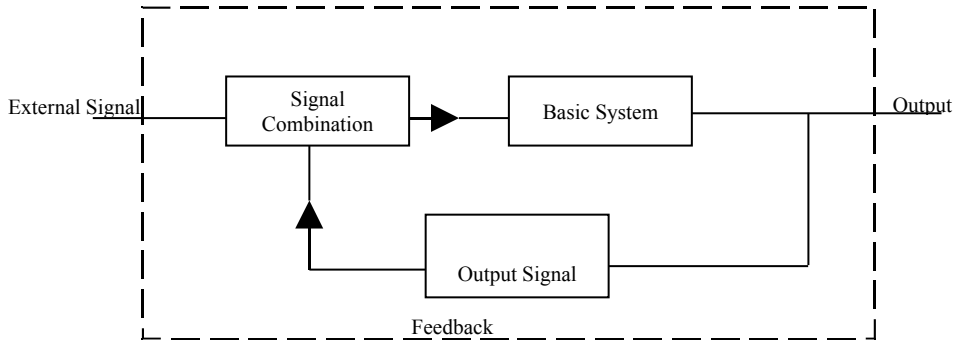


Figure 4.1: Typical Feedback system

The signal combination is usually a simple addition or subtraction. Multiplication, logical or other combination can also be used. The output signal processing is often a simple attenuation or amplitude reduction.

2.0 OBJECTIVES

At the end of this unit, students should be able to:

- be able to IDENTIFY feedback amplifier topologies
- be able to ANALYZE feedback amplifier topologies
- be able to DISCUSS the relative benefits and possible drawbacks of feedback amplifier topologies with respect to basic amplifier topologies
- be able to APPLY the concepts of feedback analysis to the DESIGN of analog amplifiers to meet or exceed stated specifications.

3.0 MAIN CONTENT

3.1 Feedback Amplifiers

A feedback amplifier consists of two parts

(i) The Amplifier system
(ii) The feedback system

The classic block diagram for a feedback system is given in figure 4.2 below.

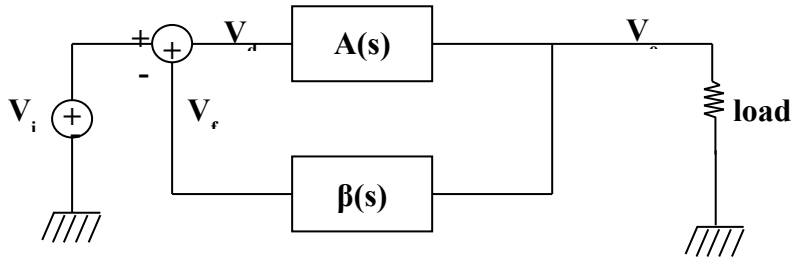


Figure 4.2: Classic feedback block system

The amplifier $A_{(s)}$ when used without the feedback is said to be in open loop with the gain denoted by A_{01}.

From the circuit in figure 4.2 above.

$Vd = Vi - Vf$ ——————————— (1)
$Vo = A_{01}Vd$ ——————————— (2)
$Vf = \beta Vo$ ——————————— (3)

From equation (2), substitute for Vd

$Vo = A_{01}(Vi - Vf)$
But $Vf = \beta Vo$

$$Vo = A_{01}(Vi - \beta Vo) \qquad (4)$$

Expand (4) and collect like terms

$$Vo = A_{01}Vi - A_{01}\beta Vo$$

$$A_{01}Vi = Vo + A_{01}\beta Vo = Vo(1 + A\beta) \qquad (5)$$

$$A_{01}Vi = Vo(1 + A_{01}\beta)$$

$$\therefore \frac{Vo}{Vi} = \frac{A_{01}}{1 + A_{01}\beta} = A_{CL} \qquad (6)$$

The Voltage gain for the closed loop is given to be

$$A_{CL} = \frac{Vo}{Vi} = \frac{A_{01}}{1 + A_{01}\beta}$$

A_{01} = open loop gain

β = feedback attenuation factor

$A_{01}\beta$ = loop gain = T

$$A_{CL} = \frac{A_{01}}{1 + T}$$

3.2 Types of Feedback Arrangements

There are two basic types of feedback arrangements and these are:

(i) Positive Feedback

In the positive feedback arrangement, the feedback voltage is in the same phase as the input voltage and it increases the input voltage amplitude. It leads to instability in systems and is only used in oscillator design.

For Positive Feedback (PFB)

$$Vd = Vi + Vf$$

$$Vo = A_{01}Vd$$

$$Vo = A_{01}(Vi + Vf) = A_{01}(Vi + \beta Vo)$$

$$Vo = A_{01}Vi + A_{01}\beta Vo$$

$$A_{01}Vi = Vo - A_{01}\beta Vo = Vo(1 - A\beta)$$

$$\frac{Vo}{Vi} = \frac{1 - A_{01}}{A_{01}\beta}$$

$$\therefore A_{CL} = \frac{Vo}{Vi} = \frac{A_{01}}{1 - A_{01}\beta} \quad \text{————PFB}$$

(ii) Negative Feedback

In negative feedback, the feedback voltage is 180^0 out of phase with the input voltage. This leads to a reduction in the input voltage and this stabilizes the system. It is used mostly in amplifier.

Negative Feedback (NFB)

$$Vd = Vi - Vf$$

$$Vo = A_{01}Vd$$

$$Vo = A_{01}(Vi - \beta Vo) = A_{01}Vi - A_{01}\beta Vo$$

$$A_{01}Vi = Vo + A_{01}\beta Vo = Vo(1 + A_{01}\beta)$$

$$\frac{Vi}{Vo} = \frac{1 + A_{01}\beta}{A_{01}}$$

$$\therefore A_{CL} = \frac{Vo}{Vi} = \frac{A_{01}}{1 + A_{01}\beta} \quad \text{————} \quad \text{NFB}$$

Both gain A and feedback β may be complex quantities having both a modulus and an angle which may depend on signal frequency.

$$A_{CL} = \frac{A_{01}\angle\theta}{1 - \beta A_{01}\angle(\theta + \phi)}$$

For NFB, T = Positive > 0

For PFB, T = Negative < 0

SELF ASSESSMENT EXERCISE

The gain and feedback factor of an amplifier at different frequencies are listed below. For each case, determine the nature of the feedback and system gain.

	F_1	F_2	F_3	F_4
A	$5000\angle 180°$	$4500\angle 160°$	$1000\angle 65°$	$500\angle 20°$
β	$0.02\angle 0°$	$0.018\angle -5°$	$1.148 \times 10^{-3}\angle -10°$	$0{,}001\angle -15°$

$$\frac{F_1}{A_{CL}} = \frac{500 < 180}{1 - 100 < 180} = \frac{5000 < 180}{101 < 180} = 49.5 < 180^0$$

Solve the rest.

From our previous discussion, the gain of an amplifier (Voltage gain) without feedback is higher than the gain with negative feedback while it is lower than the gain of the amplifier with positive feedback.
$A_{V(NFB)} < A_V < A_{V(PFB)}$.

3.3 Effect of Negative Feedback on Amplifiers

1. Gain and Gain Stability

Typical amplifiers are subject to changes such as temperature, dc supply levels and ageing. Such change results in variation in amplifier gain. Negative feedback helps to reduce the variation in gain to acceptable limits (or stabilize the gain).

For a NFB amplifier

$$A_{CL} = \frac{A_{01}}{1 + A_{01}\beta} \qquad A_{01}\beta >> 1$$

$$A_{CL} = \frac{A_{01}}{A_{01}\beta} = \frac{1}{\beta}$$

The feed back ration β is often determined by the ratio of two resistors.

Example 1

The gain of an amplifier is found to be 750 on test but under conditions of reduced dc supply and external loading, the value reduced to 400. Compare this percentage variation for the amplifier with the corresponding variation if NFB of

(a) 0.005 (b) 0.03 (c) 0.1 is used.

Solution

Percentage variation of gain without feed back is

$$\frac{original - new}{original} \times \frac{100}{1} = \frac{750 - 400}{750} \times \frac{100}{1} = 46.67\%$$

Using a β of 0.005

$$\text{The maximum gain} = \frac{A}{1 + A\beta} = \frac{750}{1 + (750 \times 0.005)} = \frac{750}{4.75} = 157.9$$

$$A\min = \frac{400}{1 + (400 \times 0.005)} = 133.3$$

$$percentage\,\text{var}iation = \frac{157.9 - 133.3}{157.9} \times \frac{100}{1} = 15.6\%$$

From this we observe that the gain of the amplifier now ranges from 157.9 to 133.3 as against the 750 to 400 and the variation is now 15.6% as against 46.7%.

Using a β of 0.03

$$A\max = \frac{750}{1 + (750 \times 0.03)} = 31.9$$

$$A\min = \frac{400}{1 + (400 \times 0.03)} = 30.8$$

$$percentage\,\text{var}iation = \frac{31.9 - 30.8}{31.9} \times \frac{100}{1} = 3.45\%$$

From the above, as the β increases, the gain reduces and the stability increases. Thus, negative feedback decreases gain but increases stability.

2. Decreased Distortion

Amplifiers exhibit a measure of non-linearity due to the curvature of the characteristic curve of active (cut off and saturation points). The non-linearity results in harmonic distortion and Clipping. Each output without distortion has a harmonic distortion component D.

$$Vout = AVin + D \quad \text{——————————} \quad (1)$$

From the feed back definition (PFB)

$Vin = Vi + \beta Vo$ ——————————— (2)

But $Vo = AVin + D$ ——————————— (3)

$\therefore Vin = Vi + \beta AVin + \beta D$ Expanding

$Vin = Vi + \beta AVin + \beta D$ Collecting like terms

$Vin - \beta AVin = Vi + \beta D$

$Vin(1 - \beta A) = Vi + \beta D$

$Vin = \dfrac{Vi + \beta D}{1 - \beta A}$ Substitute in equation 3

$Vo = A\left(\dfrac{Vi + \beta D}{1 - \beta A}\right) + D$ Taking LCM

$\dfrac{AVi + A\beta D}{1 - \beta A} + D$

$\dfrac{AVi + A\beta D + D(1 - \beta A)}{1 - \beta A} = \dfrac{AVi + A\beta D + D - A\beta D}{1 - \beta A}$

$Vo = \dfrac{AVi + D}{1 - \beta A} = \dfrac{AVi}{1 - \beta A} + \dfrac{D}{1 - \beta A}$

The term $\dfrac{AVi}{1 - \beta A}$ = actual amplified signal. $\dfrac{D}{1 - \beta A}$ = Distortion

The distortion present in the signal is reduced by a factor of (1- βA) while the desired output can be attained by controlling V_i.

When negative feedback is used, the distortion level will be reduced by a factor (1 + βA).

Example 2

In an amplifier without feedback, the gain is 36dB and the harmonic distortion at normal output level is 10%. Determine.

(a) The gain
(b) The distortion

When NFB is applied with the feedback factor of 16dB, Feedback factor = loop gain = βA

Solution

$$Acl = \frac{A}{1 + \beta A}$$ Gain (dB) = 20logA

For no feed back

$36 = 20\log A \quad \therefore A = 10^{1.8} = 63$

Feed back factor = $16 = 20\log\beta A$

$\beta A = 10^{0.8} = 6.3$

$\beta A = 6.3$ but $A = 63$

$$\therefore \beta = \frac{6.3}{63} = 0.1$$

Gain using NFB

B = 0.1

$$Acl = \frac{63}{1 + 63 \times 0.1} = \frac{63}{7.3} = 8.63$$

$20\log 8.63 = 18.7\text{dB}$

$$\text{Distortion} = \frac{D}{1 - \beta A} = \frac{0.1}{7.3} \times 100 = 1.36\%$$

3. Increased Bandwidth

Amplifiers have a frequency range over which the gain and phase shift are approximately constant. For frequencies outside the band (mid-band range), the gain falls. When NFB is applied, the gain drops. The product of the gain and bandwidth must remain constant; so as the gain drops by a factor, the bandwidth increases by that same factor.

Example 3

An RC coupled amplifier has a frequency gain of 300 and a response from 100Hz to 20KHz. A negative feedback with $\beta = 0.02$ is incorporated into the circuit. Determine the new system performance.

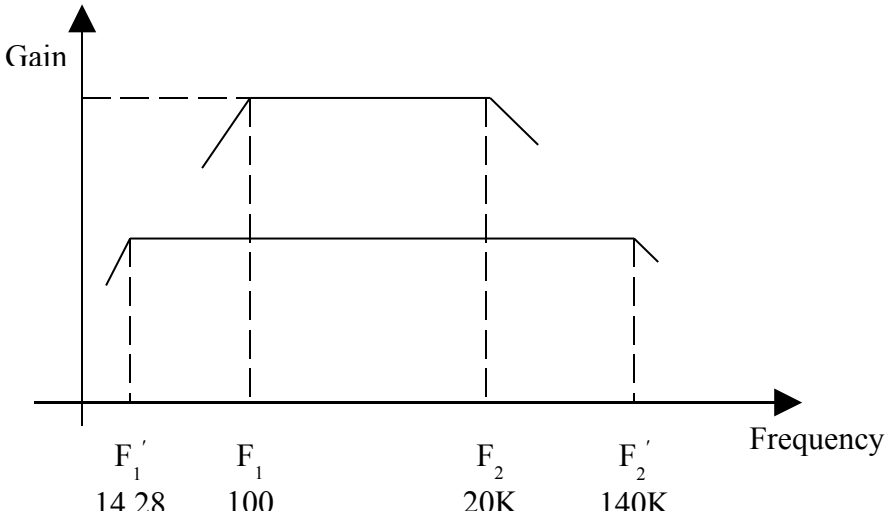
Solution

$$A' = \frac{A}{1 + A\beta} = \frac{300}{1 + 300 \times 0.02} = 42.85$$

$$f1' = \frac{f1}{1 + A\beta} = \frac{100}{1 + 300 \times 0.02} = 14.28Hz$$

$$f2' = f2(1 + A\beta) = 20KHz(7) = 140KHz$$

From the diagram



From the values above, applying the gain product bandwidth equation,

A (Bandwidth) = A′ (Bandwidth′)

A (f2 – f1) = A′ (f2 – f1′)

300 (20 KHz – 100Hz) = 42.85 (140 KHz – 14.28Hz)

5.97MHz = 5.99MHz

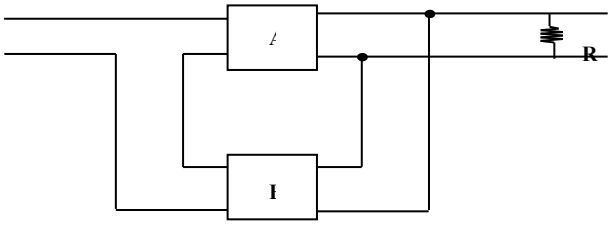
From the values above

A (f2 – f1) ≈ A′ (f2′ – f1′)

3.4 Types of Negative Feedback Circuit Topologies

There are basically 4 types of feedback amplifier circuit topologies depending on how the signals are added at the input.

1. Shunt Derived Series-Fed Feedback



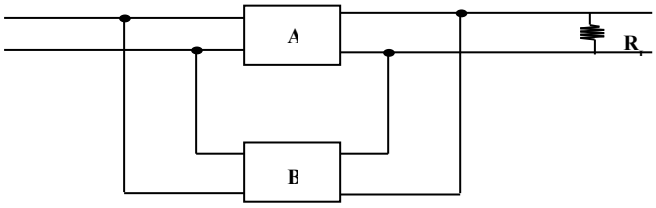
This is also known as Voltage Series Feedback. The output is connected in parallel while the input is connected in series.

The output resistance is reduced by the shunting effect of the feedback connection while the input resistance is increased by the series addition of both the feedback and amplifier resistance values.

$$Ro' = \frac{Ro}{1+\beta A}$$

$$Ri' = Ri(1+\beta A)$$

2. Shunt Derived Shunt-Fed Feedback Topology

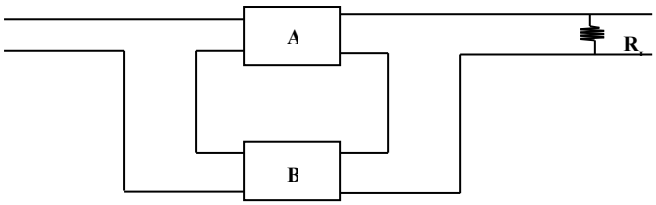


In this arrangement, the feedback is connected to both the input and output of the amplifier in parallel. This leads to a reduction in both the input and output impedance values.

$$Ro' = \frac{Ro}{1+\beta A}$$

$$Ri' = \frac{Ri}{1+\beta A}$$

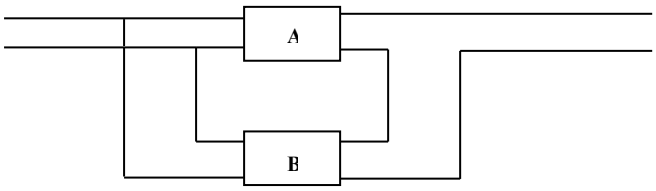
3. Series Derived Series-Fed Feedback Topology



In this arrangement, the input and output of the amplifier are connected in series. This leads to an increase in both input and output impedance.

$$Ro' = Ro(1 + A\beta)$$
$$Ri' = Ri(1 + A\beta)$$

4. Series Derived Shunt-Fed Feedback Topology



In this arrangement, the output is feedback in series and the input is connected in parallel.

The output impedance is increased by the factor 1+A β while the input impedance is decreased.

$$Ro' = Ro(1 + A\beta)$$
$$Ri' = \frac{Ri}{1 + A\beta}$$

The application of negative feedback has the following summarized effects.

(i) Decreases the effect of noise
(ii) Decreases the voltage gain
(iii) Decreases the Harmonic distortion
(iv) Increases Gain stability
(v) Increases System bandwidth

Its effect on the input and output impedance values depends on the topology used.

4.0 CONCLUSION

The advantages and applications of feed back has been studied in this unit and the different applications and advantages of the negative feedback for amplifier design has also been studied.

5.0 SUMMARY

In this unit we studied the following:

- The application of negative feed back
- The effects of negative feed back.
- The determination of the gain of a positive and negative feed back amplifier system.

6.0 TUTOR-MARKED ASSIGNMENT

(1) Determine the input resistance of a shunt input connection and the output resistance of a series output connection for a feedback amplifier.
Open loop gain = 10^5. Closed loop gain =50.Input and Output resistance of the basic amplifier are 10kΩ and 20kΩ respectively.

(2) Calculate the percentage change in the closed loop gain and a change in the open loop gain. Open loop gain = 10^5. Closed loop gain =50,β = 0.01999.Assume a change in the open loop gain is =10^4.

(3) Given a negative feedback circuit with the following parameters Open loop gain = 10^6. Closed loop gain = 100. If the magnitude of the open loop gain decreases by 20% determine the corresponding change in the closed loop gain.

7.0 REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

UNIT 2 OPERATIONAL AMPLIFIERS (OPAMPS)

CONTENTS

1.0 INTRODUCTION

The operational amplifier is a direct coupled amplifier capable of amplifying signals from DC up to a few MHz An operational amplifier —or op-amp—can perform a great number of operations, such as addition, filtering, or integration, which are all based on the properties of ideal amplifiers and of ideal circuit elements. The introduction of the operational amplifier in integrated circuit form marked the beginning of a new era in modern electronics. Since the introduction of the first IC op-amp, the trend in electronic instrumentation has been to move away from the discrete (individual-component) design of electronic circuits, toward the use of integrated circuits for a large number of applications. The majority of op-amps have three stages. The first stage converts the differential signal into a single-ended one; the second one provides the bulk on the gain and the third one the required output power.

2.0OBJECTIVES

At the end of this unit, student should be able to:

- be able to IDENTIFY op-amp circuit topologies
- be able to ANALYZE op-amp circuits
- be able to DISCUSS the relative properties of op-amp circuits.

3.0MAIN CONTENT

3.1 Ideal Op-Amp

The *Ideal Op Amp* parameters are derived to simplify circuit analysis. Op amps depart from the ideal in two ways. First, dc parameters such as input offset voltage are large enough to cause departure from the ideal.

The ideal assumes that input offset voltage is zero. Second, ac parameters such as gain are a function of frequency, so they go from large values at dc to small values at high frequencies. The table below lists the ideal opamp parameters.

Table 5.1 Ideal Opamp assumptions

PARAMETER NAME	PARAMETERS SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	a	∞

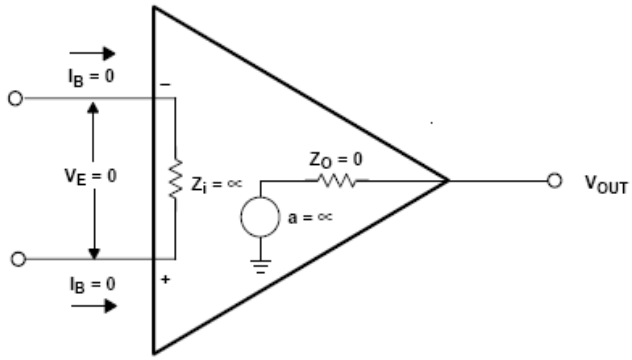


Figure 5.1 ideal Opamp

3.2 Op-Amp Configurations

There are two basic configurations of the operational amplifier and these are:

(i) The Noninverting Op Amp

The noninverting op amp configuration has the input signal connected to its noninverting input. There is no input offset voltage because VOS = VE = 0, hence the negative input must be at the same voltage as the positive input. The op amp output drives current into RF until the negative input is at the voltage, VIN. This action causes VIN to appear across RG. The voltage divider rule is used to calculate VIN; VOUT is the input to the voltage divider and VIN is the output of the voltage divider. Since no current can flow into either op amp lead.

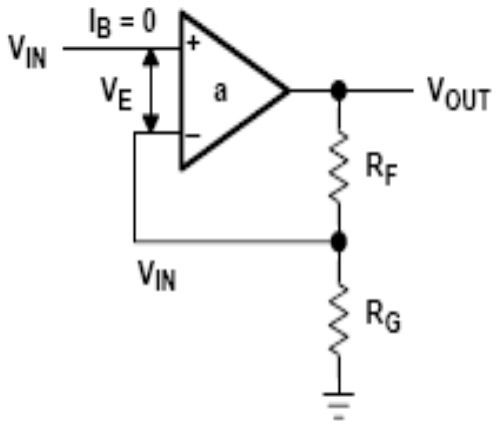


Figure 5.2 Non inverting opamp configurations

From the circuit shown in the fig above, the gain of the noninverting configuration is derived as:

$$V_{IN} = V_{OUT} \frac{R_G}{R_G + R_F}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_G + R_F}{R_G} = 1 + \frac{R_F}{R_G}$$

(ii) The Inverting Op Amp

In the inverting configuration, the input is fed through the input resistor to the inverting pin and the noninverting input of the inverting op amp circuit is grounded. One assumption made is that since the opamp has an infinite input resistance, so the feedback keeps inverting the input of the opamp at a virtual ground (not actual ground but acting like ground). The current flow in the input leads is assumed to be zero, hence the current flowing through RG equals the current flowing through RF. Using Kirchoff's law, and the Equation is written with a minus sign inserted because this is the inverting input. Algebraic manipulation gives.

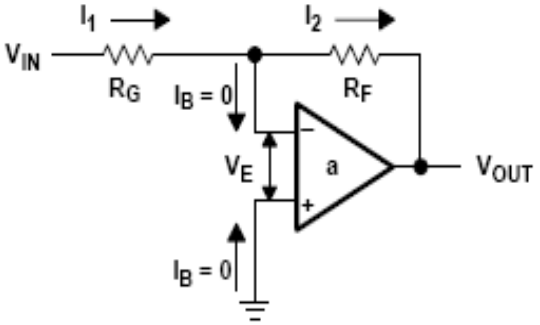


Figure 5.3 Inverting opamp configurations

From the inverting Opamp configuration the gain is derived is follows:

$$I_1 = \frac{V_{IN}}{R_G} = -I_2 = -\frac{V_{OUT}}{R_F}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G}$$

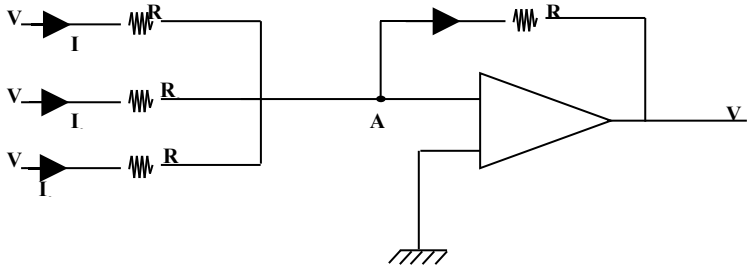
Notice that the gain is only a function of the feedback and gain resistors, so the feedback has accomplished its function of making the gain independent of the op amp parameters. The actual resistor values are determined by the impedance levels that the designer wants to establish. If RF = 10 k and RG = 10 k the gain is minus one as shown in Equation.

3.3 Applications of Op-Amps

The operational amplifier can be configured to perform mathematical operations. Some of these are listed below:

1. Adder or Summer

The adder circuit of the operational amplifier provides an output voltage proportional to the algebraic sum of the inputs, each multiplied by a constant gain factor.



$$I_1 = \frac{V_1}{R_1}, \qquad I_2 = \frac{V_2}{R_2}, \qquad I_3 = \frac{V_3}{R_3}, \qquad I_F = \frac{V_F}{R_F}$$

From Kirchoff's current law at point A

$I_1 + I_2 + I_3 = I_F$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_o}{R_F}$$

Multiply through by R_F

$$\frac{V_1}{R_1}R_F + \frac{V_2}{R_2}R_F + \frac{V_3}{R_3}R_F = -Vo$$

$$\frac{R_F}{Ri} = A_V$$

$$\therefore V_1AV_1 + V_2AV_2 + V_3AV_3 = -Vo$$

Assuming $R_1 = R_2 = R_3$

$$-Vo = \frac{V_1R_F}{R} + \frac{V_2R_F}{R} + \frac{V_3R_F}{R}$$

$$Vo = -\frac{R_F}{R}(V_1 + V_2 + V_3) = A_V(V_1 + V_2 + V_3)$$

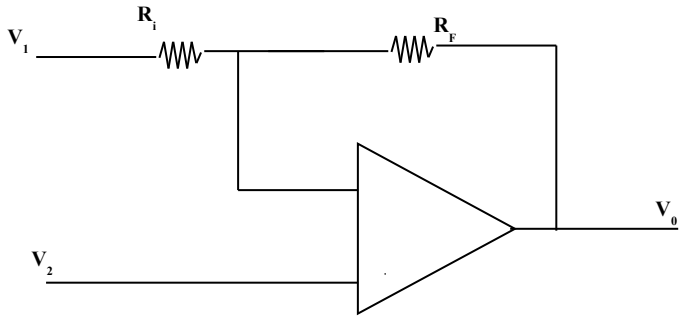
If $R_F = R$

$$Vo = -(V_1 + V_2 + V_3)$$

Hence the output is proportional to the sum of the output voltages.

2. Subtractor

The function of the subtractor is to produce an output proportional to the difference of the two input signals.



Using superposition theorem, the sum of the output with the input taken one by one is as listed below.

V_{01} = output generated by V_1

V_{02} = output generated by V_2

$$V_{01} = -\frac{R_F}{R_i}V_1$$ ——————— Inverting amplifier

$$V_{02} = \left(1 + \frac{R_F}{R_i}\right) V_2$$ ——————— Non-inverting amplifier

$R_F >> R_i$, $\frac{R_F}{R_i} >> 1$ (Rule of Thumb)

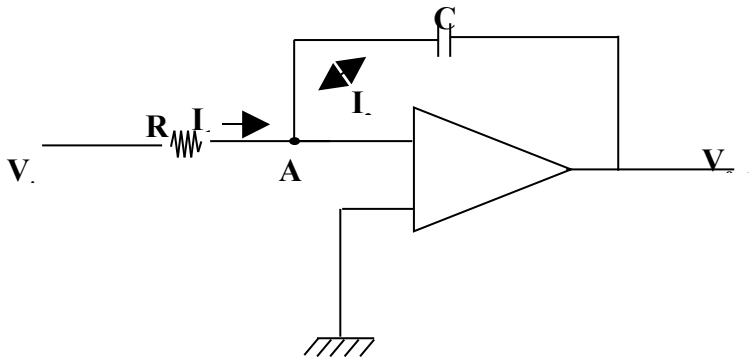
$$Vo = -\frac{R_F}{R_i} V_1 + \frac{R_F}{R_i} V_2$$

$$Vo = \frac{R_F}{R_i}(V_2 - V_1)$$

$$Vo = A_V(V_2 - V_1)$$

3. Integrator

Integration is a mathematical process of determining the area under a curve. The Op amp integrator produces an output that is proportional to the area under the curve of the input voltage.



From the concept of virtual ground, Point A = 0

$$Vin = IR \qquad \therefore I1 = \frac{V1}{R}$$

The current through the capacitor charges it in the direction shown below.

$$I_2 = -\frac{Vout}{X_C} \qquad \therefore I_1 - I_2 = 0$$

$$X_C = \frac{1}{2\pi fC} = \frac{1}{jwC} = \frac{1}{sC}$$

$$jw = s$$

$jw = s$

$$\frac{Vi}{R} = -\frac{V_{out}}{1/sC} = V_{out}sC$$

$$\therefore Vout = -\frac{Vi}{sRC}$$

Voltage gain = $\frac{Vo}{Vi} = -\frac{1}{sRC}$

Converting this to time domain

$$Vo = -\frac{1}{RC}\int_0^t Vi(t)dt$$

Alternatively

$I_1 = I_2$ where I_2 = Current through the capacitor

$$I_2 = C\frac{dVc}{dt} \quad \text{but } Vc = Vo$$

$$\frac{dVc}{dt} = \frac{I_2}{C} \qquad \text{but } I_1 = I_2 = -\frac{Vi}{R}$$

$$\frac{dVout}{dt} = -\frac{V_1}{RC} \qquad \therefore dVout = -\frac{V_1}{RC}dt$$

Integrating both sides

$$Vout = -\frac{1}{RC}\int_0^t Vidt$$

The integrator is a low pass filter and produces more output for low frequency signals.

Example 1

A 5V, 1KHz sinusoidal signal is applied to the input of an op amp integrator. R = 100K, C = 1μF, determine the V_{out}.

$V_{in} = 5 \text{ Sin } 2\pi ft = 5 \text{ Sin } 2000\pi t$. Integration is from t = 0 to t = t

$$Vo(t) = -\frac{1}{RC}\int Vin(t)$$

$$-\frac{1}{RC} = -\frac{1}{100 \times 10^{3} \times 1 \times 10^{-6}} = -10$$

$$Vo = -10\int_{0}^{t} 5Sin200\pi t = -50\left[-\frac{Cos2000\pi t}{2000\pi}\right]_{0}^{t}$$

$$= \frac{1}{40\pi}(Cos2000\pi - 1)$$

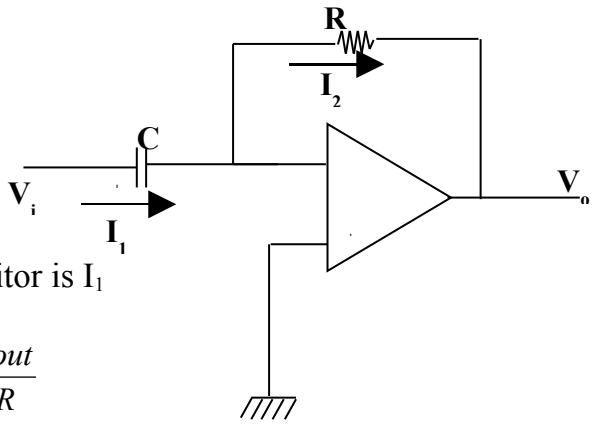
4. Differentiator

This is the process by which the rate of change of a curve at any given point can be determined. It is essentially the inverse of integration.

$$Vin = I_1 X_C \qquad \therefore I_1 = \frac{V_{in}}{X_C}$$

$$I_2 = -\frac{Vout}{X_C} \qquad I_1 = I_2$$

$$\frac{Vin}{X} = -Vout$$



But the current through the capacitor is I_1

$$\therefore I_1 = C\frac{dV_{in}}{dt} \qquad \therefore C\frac{dV_{in}}{dt} = -\frac{Vout}{R}$$

$$Vout = -RC\frac{dV_{in}}{dt}$$

The differentiator is basically a high pass filter.

4.0CONCLUSION

In this unit you have been introduced to the operational amplifier and its applications.

5.0SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of operational amplifiers and the basic configurations of op amps.

6.0 TUTOR-MARKED ASSIGNMENT

A 5V, 10 KHz sinusoidal signal is applied to the input of an op amp integrator for 10 seconds. R = 100K, C = 1μF, determine the V_{out}.

7.0REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

MODULE 3

Unit 1 DC Power Supplies
Unit 2 Voltage Regulators
Unit 3 Heat Sinks

UNIT 1 DC POWER SUPPLIES

CONTENTS

1.0 INTRODUCTION

The DC power supply is a circuit design of provide DC power supply mostly for the powering of portable devices. The most common source of dc power supplies are batteries but they are faced with the following challenges:

- Limited life
- Reduction in terminal voltage over time
- Limited capacity

2.0 OBJECTIVES

At the end of this unit, students should be able to:

- to introduce the students to the principles of DC power supply systems
- to introduce students to the component parts of the DC power supply
- to introduce student to the design of Dc power supplies and voltage regulators.

3.0 MAIN CONTENT

3.1 DC Power Supply

There are two types of DC power supply. These are:

- **Unregulated Power Supply**: This is a power supply whose terminal voltage is affected significantly by the amount of load. As the load draws more current the DC terminal voltage becomes less.
- **Regulated Power Supply**: This DC power supply has a terminal voltage which remains constant regardless of the amount of current drawn from it. A regulated power supply is achieved by the addition of a voltage regulating circuit to an unregulated DC power supply.

Examples of voltage regulators are:

1. Zener diode voltage regulators
2. Transistor series voltage regulator
3. Integrated circuit voltage regulators both adjust able types and the fixed types. (e.g. 7805, 7808, e.t.c., LM 317, 117)

The block diagram of a typical dc power supply system is given below:

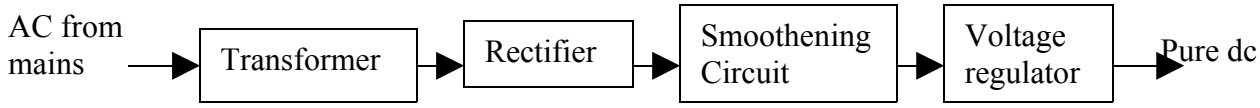


Fig 6.1: Components of a DC Power Supply

3.2 Components of a Typical DC Power Supply System

(i) The Transformer

The transformer is responsible for stepping down the voltage level of incoming ac mains supply. There are basically two classes of transformers. These are:

- The step-up transformer – This steps up the voltage from the ac mains. Its output voltage is higher than the input voltage level.
- The step-down transformer – This is a reverse of the step-up transformer and its output voltage level is lower than the input voltage.

The dc power supply utilizes the step down transformer.

(ii) Rectifiers

The purpose of the rectifier is to convert the AC signal from the transformer to DC. There are also two classes of rectifiers and these are:

- The half wave rectification
- The full wave rectification

Under the full wave rectification we have:

- Center tapped transformer full wave rectification
- The bridge rectifier full wave rectification

3.3 Half Wave Rectifier

The circuit below shows the basic half wave rectifier circuit and the corresponding wave form.

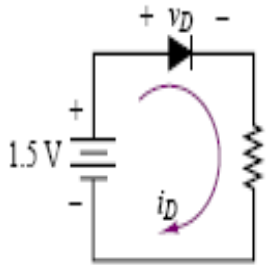


Fig 6.2: Half wave rectifier

The rectification is achieved by the use of a single diode due to the diode's characteristics of conducting in one direction only in forward bias (forward bias).

Mode of Operation

During the positive half cycle of the input AC Voltage the diode D is forward biased and it conducts assuming the voltage peak is much grater than 0.6V (diode drop for silicon) the voltage and current of the load flow but during the negative half cycle, the diode is reversed biased and does not conduct thus V_1 and 1, are zero thus the output of the half wave rectifier is a pulsating DC voltage which is used only in battery charging.

The frequency of the ripple is the same as that of the input voltage. When this output is measured by a DC meter we get the average positive value for both voltage and current. The half wave rectifier converts the sinusoidal wave form with an average value of zero to a unidirectional wave form with a non zero average waveform. The wave forms for the half wave rectifier is displayed in the figure below.

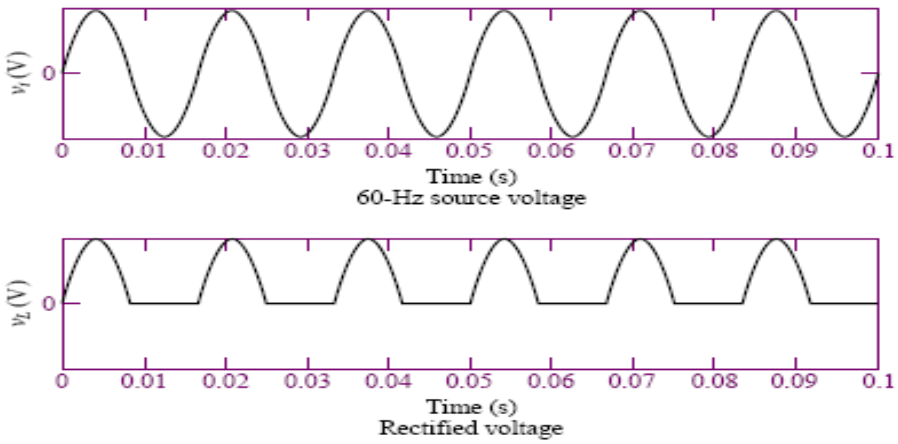


Fig 6.3: Half wave rectifier wave forms

Figure half wave rectifier input/output wave forms.

$V_i = Vm \sin Wt$ Instantaneous voltage

R_F And R_l being forward resistance and load resistance

$I_m = \frac{V_m}{Rf+Rl}$

I_M And V_m are peak values

The DC ammeter is connected to indicate the average value of current passing through it. Mathematically the average current Idc is an integration of the instantaneous current over the half cycle.

$$Idc \neq \frac{1}{2\pi}\int_0^{\pi} i\, dx$$

$i = Im \sin X$

$$I\ dc = \frac{1}{2\pi}\int_0^{\pi} Im \sin X\ dx = \frac{Im}{\pi}$$

$$I\ dc = \frac{Im}{\pi}$$

The AC meter on the other hand reads the effective or rms value of the current passing through it. Mathematically, the rms value squared which is the area of one cycle of the curve divided by the base is given by

$$(Irms)^2 = (\frac{1}{2\pi}\int_0^{2\pi} I^2\, dx)\ full\ circle$$

For half wave

$$(I_{rms})^2 = (\frac{1}{2\pi}\int_0^{2\pi} {I_m}^2 \, sin^2 \; x \; d \; \&)^{\frac{1}{2}} = \frac{I_m}{2}$$

Therefore $I_{rms} = \frac{I_m}{2}$ = rms value of load current the V_L (dc) or load voltage is also derived in as similar manner.

$$V(dc) = \frac{V_m}{\pi} = average \; value \; (dc)$$

Where $V_m = peak \; value \; of \; load \; voltage$

3.4 Efficiency of Rectifiers

The efficiency of rectification is given by the ratio of the output DC power to the total amount of input power supplied to the circuit. It is also called the conversion efficiency.

$$EFF = \frac{P_{dc}}{P_{in}} = \frac{power \; in \; the \; load}{input \; power}$$

$$P_{dc} = I(dc^2) \; R_l = \frac{(I_m)^2}{\pi} R_l = \frac{{I_m}^2}{\pi^2} R_l$$

$P_{in} = Idc^2(R_l + R_o) where \; R_o = R_f + R_s$

R_s = transformer secondary winding resistance

$P_{in} = {I_m}^2 \; (R_l + R_o) = \; the \; current \; at \; the \; secondary \; transformer \; is \; measured \; in \; rms$

$$= I_{rms} = \frac{I_m}{2}$$

$$P_{in} = (\frac{I_m}{2})^2 \; (R_l + R_o) = \frac{{I_m}^2}{4} \; (R_l + R_o) = \frac{P_{dc}}{P_{in}}$$

$$= \frac{\frac{{I_m}^3}{\pi^2} R_l}{\frac{{I_m}^2}{4} \; (R_l + R_o)} = \frac{4 \; (R_l)}{\pi^2 \; (R_l + R_o)}$$

Dividing up and down by R_l

$$\frac{4}{\pi^2 \; (1 + \frac{R_o}{R_l})} = \frac{0.406}{1 + \frac{R_o}{R_l}} \times 100$$

If R_o is neglected, the efficiency becomes 40.6%. This is the maximum possible efficiency of the half wave rectifier. The frequency of the half wave rectifier output is the same as that of the AC input.

Peak Inverse Voltage

It is the maximum voltage the diode has to withstand without failing when it is non conducting. For the half wave rectifier it is V_m.

Ripple Factor

This is a measure of the AC components (fluctuating components) present in the rectifier output. It is given by:

$$= \frac{value\ of\ alternating\ components\ of\ the\ wave}{average\ value\ of\ the\ wave}$$

$$r = \frac{I_{rms}}{Idc} = \frac{V_{rms}}{Vdc}$$

$$\frac{I_{rms}}{I_{dc}} = \frac{\frac{I_m}{2}}{\frac{I_m}{\pi}} = \frac{\pi}{2} = 1.57$$

$$Y = \sqrt{(1.57)^2} = 1 = 1.21$$

This shows that the rms ripple exceeds the DC output voltage and thus the half wave rectifier is a poor rectifier circuit.

Voltage Regulation

This is the variation of DC output voltage as a result of variation of the DC load current.

$$\%regulation = \frac{V_{noload} + V_{full\ load}}{V_{full\ load}} \times 100\%$$

When there is no load no output current flows, but when the output current flows there is a drop over Rs and RF. (R_f = diode forward resistance and R_s = transformer secondary resistance winding.)

$$V_{fl} = V_{NL} \frac{R_l}{R_{o+} R_L} \quad where\ R_o = R_s + R_f$$

Substituting V_{FL} above with the VR equation we have

$$VR = \%regulation = V_{NL} - \frac{\frac{V_{NL}R_l}{R_o + R_l}}{\frac{V_{NL}R_l}{R_o + R_l}}$$

$$VR = \frac{R_o}{R_l}$$

Example 1

A half wave rectifier using a silicon diode has secondary E.M.F of 14.14 Vrms with a resistance of 0.2. The diode forward resistance is 0.05 and its threshold voltage is 0.7V. If the load resistance is 10, determine (i) DC load current (ii) DC load voltage (iii) VR (iv) Efficiency

$$V_m = \sqrt{2} \times V_{rms} = \sqrt{2} \times 14.14 = 20V$$

$$R_o = R_s + R_f = 0.2 + 0.05 = 0.25$$

i. $$I_m = \frac{dc\ V_m - diode\ threshold\ voltage}{R_o + R_l} = \frac{20-0.7}{0.25+10} = 1.88$$

$$Idc = \frac{I_m}{\pi} = \frac{1.88}{\pi} = 0.6A$$

ii) $$V_l(dc) = I_l(dc)R_l = 0.6 \times 10 = 6V$$

iii) $$V_o = \frac{R_o}{R_l} = \frac{0.25}{10} = 2.5\%$$

iv) $$eff = \frac{40.6}{1+\frac{R_o}{R_l}} = \frac{40.6}{1+\frac{0.25}{10}} = 39.6\%$$

3.5 Full Wave Rectifier Center Tapped

In this case both half cycles are utilized with the help of two diodes working alternatively. For full wave rectification the use of a transformer is essential but it is optional in the half wave rectification.

Operation

When the input is switched on, the ends of the transformer M and N become positive and negative with the mid point (center tap) at zero potential. So when D_1 is forward biased, D_2 conducts through the load back to the center tap. When the polarities of M and N are interchanged, D_1 becomes forward biased and D_2 reversed. D_1 then conducts allowing current to flow through the load to the center tap. From this we realize that D_1 and D_2 are actually half wave rectifiers but since they conduct alter negatively through the same load, the load sees a full wave rectified output.

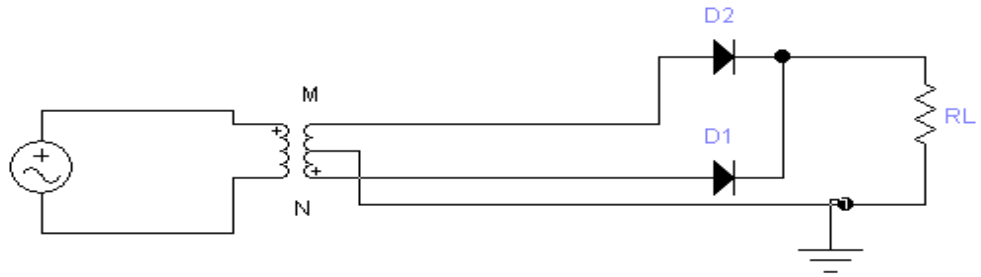


Fig 6.4: Full wave rectifier center tapped

The rms value of the output voltage $= \frac{V_m}{2}$.

The average value of the DC voltage is derived from the equation below

$$V_l(dc) = \frac{2V_m}{\pi} = 0.636V_m$$

$$I_l(dc) = \text{ or } I_{dc} = \frac{2I_m}{\pi}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$I_m = \frac{V_m}{R_f + R_l} \text{ where } R_f \text{ is diode forward drop and } R_l \text{ is load resistance}$$

$$eff = \frac{P_{dc}}{P_{in}}$$

Remember P = VI = I^2R since V = IR

$$R_o = R_f + R_s$$

In computing for P_{dc} we make use of the average or DC value of the circuit.

$P_{dc} = I_l\,(R_o + R_l)$

$I_l = (\frac{2I_m}{\pi})$

$P_{dc} = = \left(\frac{2I_m}{\pi}\right)(R_l) = \frac{4{I_m}^2}{\pi^2}\,(R_l)$

$P_{in} = {I_{rms}}^2\,(R_o + R_l)$. For Pin we make use of the rms value of current.

$I_{rms} = \frac{2I_m}{\sqrt{2}}$

$P_{in} = \left(\frac{{I_m}^2}{\sqrt{2}}\right)(R_o \neq R_l) = \frac{{I_m}^2}{2}\,(R_o + R_l)$

$\frac{P_{dc}}{P_{in}} = \frac{8\,R}{\pi^2(R_o + R_l)} = \frac{0.812}{(1 + \frac{R_o}{R_l})} = \frac{81.2\%}{1 + \frac{R_o}{R_l}}$

It is twice the value of the half wave circuit. This is because both half cycles of the input wave are used. It can also be seen that the frequency of the output is twice that of the input.

Ripple Factor

As derived earlier, ripple factor is the ratio of the rms value of AC components of the output to the DC value of the load voltage:

$= \frac{I_{rms}}{I_{dc}} = \frac{V_{rms}}{V_{dc}}$

We came to the point where r = $\sqrt{(\frac{{I_{rms}}^2}{I_{dc}} - 1)}$

$I_{rms} = \frac{I_m}{\sqrt{2}}$; $I_{dc} = \frac{2I_m}{\pi}$

$therefore\ \frac{I_{rms}}{I_{dc}} = \frac{\pi}{2/_2} = 1.11$

$\& = \sqrt{((1.11)^2 - 1)} = 0.482$

This shows that the ripple factor has dropped to 0.482 from 1.21 for the half wave.

Peak Inverse Voltage

In the center tap transformer we realize that at the point when D_1 is contributing, D_2 is not because at that point the N is at a negative potential. If our transformer is a 9 volt center tap is 9 volts. If D_1 is conducting with the center tap at 0 volts. The voltage difference between D_1 and $D_2$is from +9V to -9 volts which is 18 volts. Thus the diode must be able to withstand 18V or 2 times the V peak.

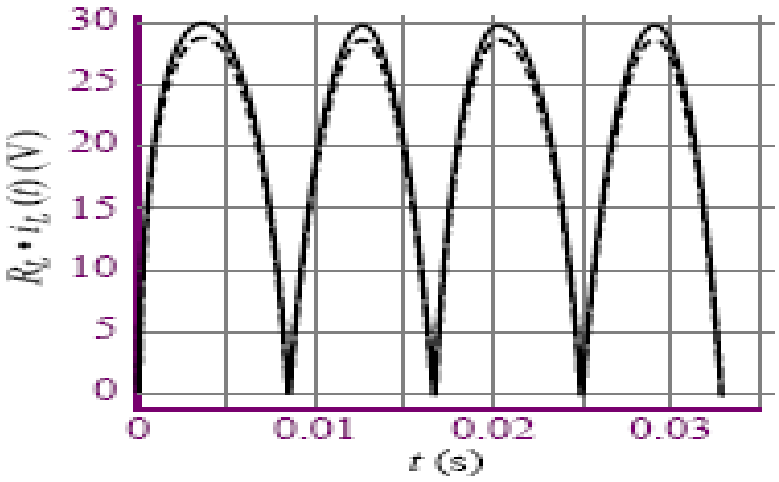
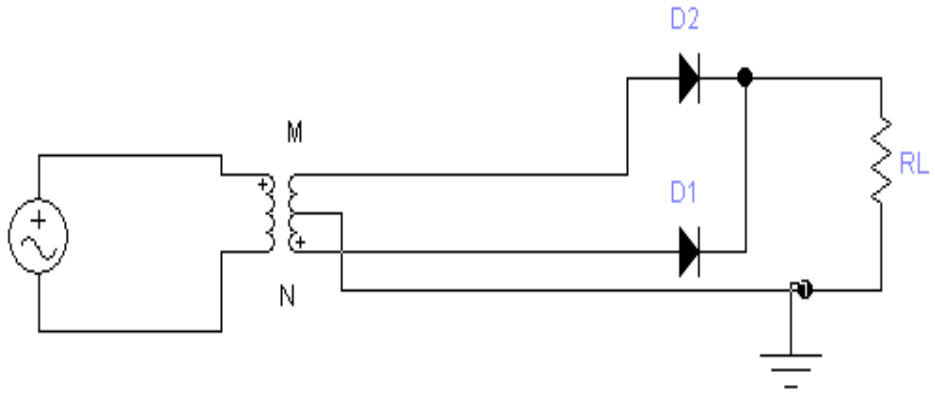


Fig 6.5: Full wave rectifier center tapped wave forms

Example 2

From the full wave rectifier shown below determine

- The peak, rms values of load voltage
- The peak, rms values of load current
- The ripple factor
- Peak and average diode currents
- Total power supplied to the load



Solution

K = Transformer ratio

$peak\ of\ the\ primary = V_{rms} \times \sqrt{2}$

$= 220 \times \sqrt{2} = 312V$

From the transformer ratio the peak voltage of secondary $= \frac{312}{2} = 156V$

$V_{MG} = V_{GN} = \frac{156}{2} = 78V$

1. Peak value of the load voltage = 78V
   Average value of the load voltage = $\frac{2V_m}{\pi} = 49.6V$
   Rms value of load voltage = $\frac{V_{peak}}{\sqrt{2}} = 55V$

2. Peak value of load current = $\frac{V_p}{R_l} = \frac{peak\ value\ of\ load\ voltage}{load}$

   $I_p = \frac{78}{100} = 0.78A$

   $I_{dc} = average\ value\ of\ load\ current = \frac{2V_m}{\pi} = \frac{2 \times 0.78}{\pi} = 0.496A$

   $I_{rms} = rms\ value\ of\ load\ current = \frac{I_{peak}}{\sqrt{2}} = 0.55A$

3. Ripple factor = $\sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\frac{0.55^2}{0.496} - 1} = 0.48$

4. Peak diode current = peak load current = 0.78
   Average diode current = $\frac{I_{D\,(max)}}{\pi} = \frac{I_p}{\pi} = \frac{0.78}{\pi} = 0.25A$
   Since each diode conducts for one load

5. Total power supplied to the load
   P = $V_{rms} \times I_{rms} = 55 \times 0.55 = 30.25W$

3.5 Full Wave Bridge Rectifier

It is the most frequently used rectifier circuit for electronic DC power supplies. It requires four diodes but the center tapped transformer is not required. It comes in 3 distinct physical forms:

1) Four discrete diodes
2) As a part of an array of diodes in an IC
3) One devices inside a four terminal case diagram

Mode of Operation

During the positive input half cycle the M terminal is positive with this, diode one and diode three become forward biased (conducting) while the diode two and diode four are reversed biased. The direction of current flow is indicated in diagram A. while when N becomes positive with respect to M, diodes one and three become reversed biased and diodes two and four become forward biased. The current flow is illustrated in the diagrams below

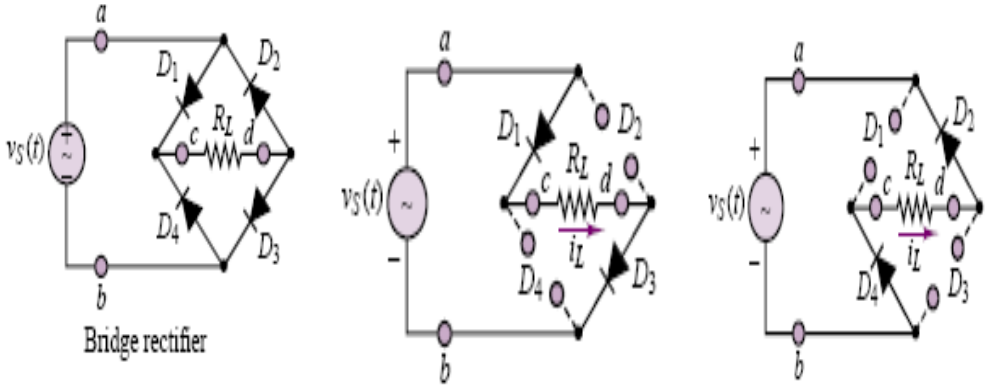


Fig 6.6: Full wave bridge rectifier

The current flow through the load in one direction with point A acting as the anode and point C the cathode the output frequency is twice that of the input wave form because both halves of the input wave form are utilized and each diode has a peak inverse voltage of magnitude equal to the peak of the transformer secondary voltage or current. The rms and average values are the same as that of the center tap. The ripple factor is also the same at 0.482.

3.7 Smoothing Circuits

The easiest way to smooth a circuit is by adding a capacitor in parallel to the resistive load. Instantaneous voltage across the capacitor and the load during diode cut off is given by:

$V_l = (V_{pk} - V_D)\frac{e^{-1}}{CR_l}$. $CR_l = time\ constant.$ It is much greater than the period of the supply wave form. The output of the DC consisting $V_{dc} + V_{ripple} = V_{pk} - V_D$. The bigger the capacitance the better the smoothing.

Capacitor Filter

During the positive half, the capacitor charges and when the input voltage begins to drop the capacitor maintains the charge and discharges through the $R_l$reverse biasing the diode. The rate the discharge is determined by R_lC-time constant. The larger the time constant, the less the capacitor will discharge and the higher the R_lC the lower the ripple. The variation in the output voltage during charging and discharging is known as the ripple.

Ripple factor is an indication of effectiveness of the filter and it is defined as rms ripple voltage.

$$r = \frac{V_r}{V_{dc}}$$

The lower the ripple factor the better the filter

From the diagram, $Vc = Vp(in)\ell^{\frac{\tau}{RC}}$ exponential decay

Since the discharge time for the capacitor from one peak to the next approximately tends to T when V_c reaches its minimum value.

$$Vc = Vp(in)\ell^{\frac{\tau}{RC}}$$

Since RC tends to T (for improved filtering and reduced ripple $\frac{T}{RC}$ becomes less than 1).
Therefore $e^{\frac{T}{RC}} = 1 - \frac{T}{RC}$

Therefore

$$Vc(\min) = Vp(in)\ell^{\frac{\tau}{RC}} = Vp(\min)(1 - \frac{\tau}{RC}$$

Peak ripple voltage $V_{r(pp)} = V_{p(in)} - V_{r(min)}$

$$V_{r(pp)} = \frac{V_{p(in)}\ T}{RC} = but\ T = \frac{1}{f}$$

$$V_{dc} = V_{p(in)} - V_{r(peak)}\ but\ V_{r(peak)} = \frac{V_{r(pp)}}{2}$$

$$V_{dc} = V_{p(in)} - \frac{V_{r(pp)}}{2} = V_{p(in)} = \frac{V_{p(in)T}}{2RC}$$

$$V_{dc} = (1 - \frac{T}{2RC})V_{p(in)}$$

Peak ripple voltage $= \frac{V_{r\ (pp)}}{2} = \frac{V_{p\ (in)T}}{2RC}$

Since the ripple waveform is a saw tooth diode $V_{r(p)}\ by\ \sqrt{3}$ to convert peak to rms.

$$V_{(rms)} = \frac{V_{p(in)T}}{2RC} \times \frac{1}{\sqrt{3}}$$

$$V_{(rms)} = \frac{V_{p(in)T}}{2RC} . \frac{1}{\sqrt{3}}$$

Example 3

Determine the ripple factor for the filtered bridge rectifier. Vrms = 115V

$$= \frac{V_p}{\sqrt{2}} = V_{rms}$$

$$V_p = 115 \times 1.414 = 162.6V$$

V secondary = $\frac{162.6}{10} = 16.26V$

$$V_{p(in)} = V_{fsc} - 2 \times voltage\ drop = 16.26 - 1.4V = 14.86V$$

Filtered $V_{dc} = \left(1 - \frac{T}{2RC}\right) V_{p(in)}; \quad T = \frac{1}{F}; F = 120$

$$= \left(1 - \frac{1}{2 \times 120 \times 22 \times 10^3 \times 5 \times 10^{-6}}\right) 86F = 120HZ = 14.3volts$$

Rms ripple voltage = $\frac{V_{r\,(peak)}}{\sqrt{3}}$

$$V_{r(peak)} = \frac{V_{r(pp)}}{2}$$

$$V_{r(pp)} = \frac{V_{p(in)}}{2RC}$$

$$V_{r(p)} = \frac{14.86 \times 1}{22 \times 10^3 \times 5 \times 10^{-6} \times 120 \times 2} = \frac{14.86}{264} = 0.56$$

$$V_{r(rms)} = \frac{0.56}{\sqrt{3}} = 0.324V$$

Ripple voltage= r = $V_{r(rms)} = \frac{0.324}{14.3} = 0.0226 = 2.27\%$

The average value of the voltage from the full wave rectifiers is twice that of the half wave. Thus,

$$Vdc = \frac{2(Vpk - Vd)}{\pi} = 0.3185(Vpk - Vd)$$

The half wave rectifier is the simplest but its average dc voltage output is low and it has a large amount of ripple which has a frequency equal to the input frequency.

The full wave (centre tapped and bridge circuits) have a higher output voltage with reduced ripple. Its ripple has a frequency that is twice the value of the input voltage frequency. It requires diodes with twice the PIV (Peak Inverse Voltage) rating. Thus PIV = $2V_{peak}$ for the centre tapped arrangement.

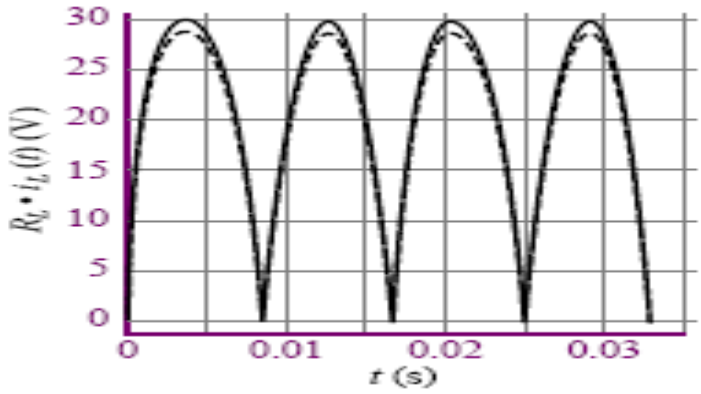


Figure 6.8 Full wave output waveforms

Example 4

Find the peak value of the ripple voltage in a half wave rectifier when the peak output voltage is 20V. R_L = 250 Ω and C = 1250uF, f = 50 Hz.

Vripple (peak) = $\frac{I_L}{2FC}$

Vout = 20V, R_L = 250,

IL = $\frac{20}{250} = 80mA$

Vr(pk) = $\frac{80 \times 10^{-3}}{2 \times 50 \times 1250 \times 10^{-6}} = 0.64V$

The Vdc = Vpk – Vr(pk), therefore for the first condition with C = 1250uF,
Vdc = 20 – 0.64 = 19.36V

The formula for calculating the needed capacitance to produce a specified ripple factor is given below:

$let\ V_{dc} = V_{p(in)}$

$r = \frac{V_{r(rms)}}{V_{dc}}$

$V_{r(rms)} = \frac{V_{p(in)T}}{\frac{2RC}{3}}$

For T = 1/F= 1/100 full wave, $V_{p(in)} = V_{dc} = \frac{V_{p(in)T}}{\frac{2RC}{3}}$

$r = \frac{0.0024}{RC}$

4.0 CONCLUSION

In this unit you have been introduced to the basic principles of the DC power amplifier, its applications and the design procedure.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of the Dc power supply and have been able to derive the different parameters of the DC power supply circuit.

6.0 TUTOR-MARKED ASSIGNMENT

(1) Find the peak value of the ripple voltage in a half wave rectifier when the peak output voltage is 20V. R_L = 250 Ω and C = 5000uF, f = 50 Hz.

(2) A single phase full wave rectifier supplies power to a 1KΩ load. The AC voltage applied to the diodes is 300-0-300 Vrms. If the diode resistance is 25 and that of the transformer is negligible, determine (i) Average load current (ii) Average value of load voltages (iii) Rms value of the ripple (iv) Efficiency

7.0 REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

UNIT 2 VOLTAGE REGULATORS

CONTENTS

8.0 INTRODUCTION

A voltage regulator is a circuit or device that provides a well specified, constant and stable DC voltage supply to other circuits. The output voltage is controlled by internal circuitry and is relatively independent of the current supplied by the regulator.

9.0 OBJECTIVES

At the end of this unit, student should be able to:

- identify voltage regulator circuits
- analyze the different voltage regulator circuits
- design voltage regulator circuits with the relevant protection circuits.

10.0 MAIN CONTENT

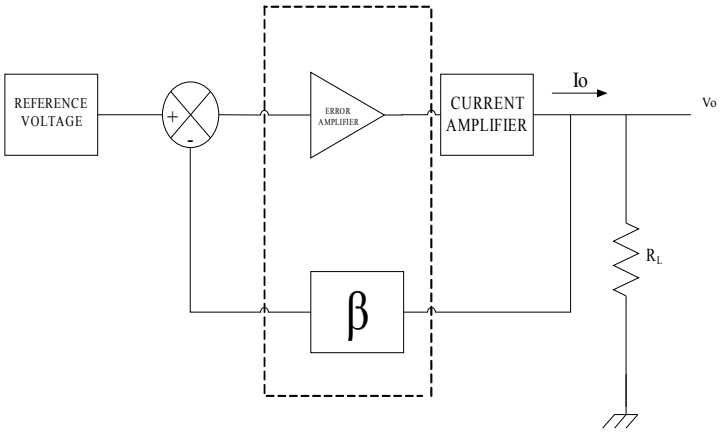
3.1 Introduction to Voltage Regulators

Voltage regulators are circuits incorporated into the unregulated DC power supply circuits and the ensure that the terminal voltage remains unchanged regardless of the variations in the input voltage provided the operational limits are not exceeded There are DC power classified as either:

1. series regulators
2. shunt regulators
3. switching regulators

The basic diagram of a voltage regulator is shown below to consist of:

- A reference voltage circuit
- An error amplifier
- Current amplifier



3.2 Voltage Regulators Figure of Merit

Variations in the reference voltage can be caused by variations in the power supply voltage and this affects the output voltage. This parameter known as line regulation is defined as ratio of change in output to a given change in input supply voltage.

$$\text{Line regulation} = \frac{\Delta Vo}{\Delta V^{+}}$$

Output resistance is defined as the rate of change of output voltage with output current.

$$R_{of} = - \frac{\Delta Vo}{\Delta Io}$$

The change in Vo and Io is as a result of change in R_L with other parameters remaining constant.

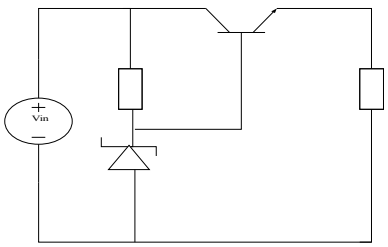
Load Regulation: This is the change in output voltage between no load current condition and full load current condition, expressed in percentage.

$$\text{Load regulation} = \frac{Vo(noload) - Vo(full\_load)}{Vo(noload)} \times 100\,\%$$

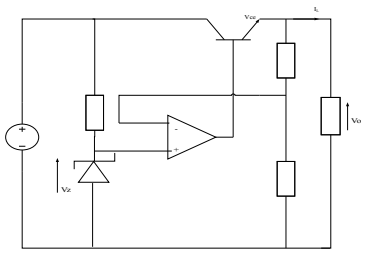
3.3 Series Pass Regulators

Series regulators control or maintain a constant dc voltage output by continuously adjusting the voltage drop across a power transistor connected in series between the unregulated input and the load. The transistors are biased in the linear region and as such are also called linear regulators.
They however are inefficient because a large amount of power is wasted in the pass transistor and they require big transformers and capacitors to scale the time voltage and filter it.

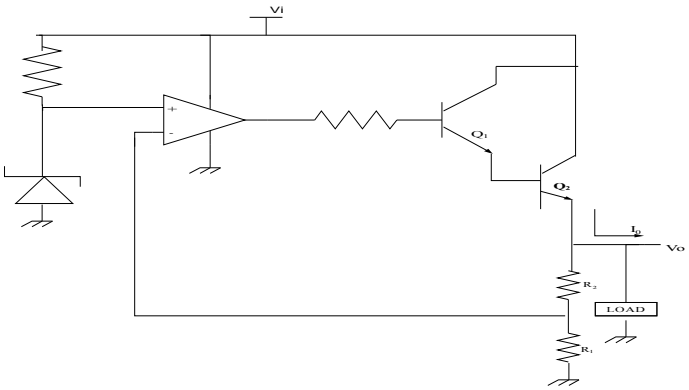
The figure below shows a simple series pass voltage regulator



or



This circuit can also be redrawn with a Darlington pair as the pass transistor for higher current.



The basic building blocks of the voltage regulator include:

- **The Voltage reference**: This provides a scaled version of the input which is stabilized by the Zener diode.
- **The Error amplifier**: This takes a scaled version of the output and compares it with the reference voltage and adjusts Vo via the series pass transistor.

$$\text{Vn} = \frac{VoR1}{(R1 + R2)} \qquad \text{Vp} = \text{Vref}$$

The error signal Vd= Vp – Vn.

The aim of the error amplifier is to drive the pass transistor in such a way that if the Vo is increasing, the transistor will reduce its amplification and if Vo is decreasing, the transistor will increase its amplification such that Vo is kept constant.

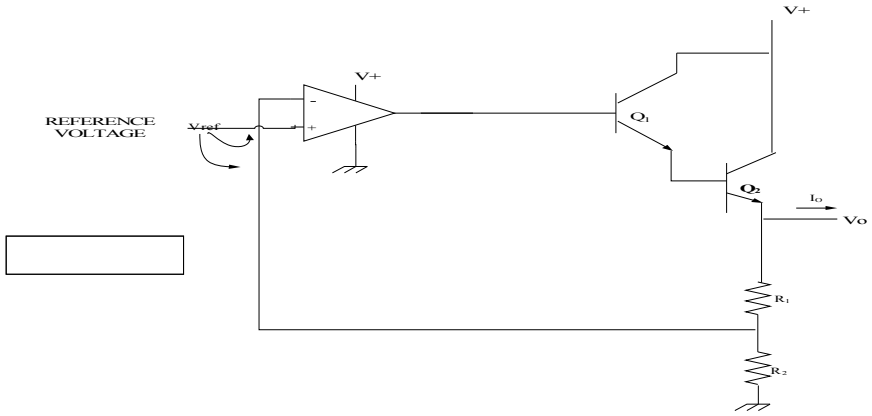
- The feedback network series to scale Vo to a value suitable for comparison against Vref by the error amplifier,

$$\text{Vo} = \left(1 + \frac{R2}{R1}\right) Vref \quad \text{(Non- inverting OP AMP)}$$

But Vref is fixed, so the only way to control Vo is by altering R_2/ R_1.

- The Series Pass element: The function of this is to boost the output current capabilities of the error amplifier. It transfers large current to the load under the supervision and control of the error amplifier. NPN transistors are mostly used for this.

From the circuit given below:



From our equation,

$$\text{Vref} = \frac{VoR2}{R1 + R2} \text{ Potential divider}$$

$$\text{Vo} = \text{Vref}\ \frac{Vref\,(R1 + R2)}{R2}$$

The open loop output resistance is the output resistance of the Series Pass transistors operating in the emitter follower configurations.

From the circuit diagram,

The NPN BJT generates a collector circuit β times as large as that entering the base terminal. $Ic = \beta I_B$

And releases both Ic and I_B to the Emitter.

$I_E = Ic + I_B$, therefore $IE = (\beta + 1)I_B$

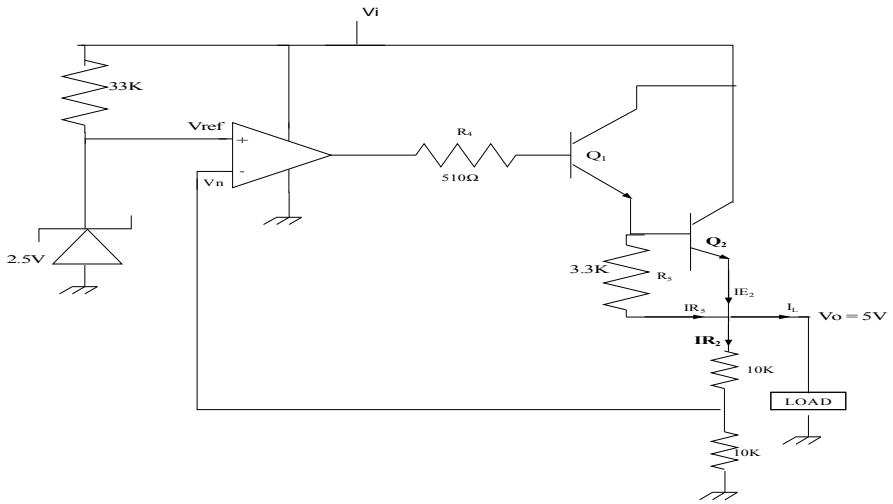
For low Power BJTs, $V_{BE\,(ON)} \simeq 0.7$ and $\beta \simeq 100$ or more but

For Power Transistors, $V_{BE\,(ON)} \simeq 1V$ and β is in the range of 10s.For this reason, Darlington pairs are used to give β of the range of 1000s or more.

Example 1

From the circuit below:

(a) Determine the voltage and current at the OP AMP output
(b) Find the minimum value of Vi at which the circuit will still function properly.



RL = 1Ω

$V_{BE1} = 0.8$ $V_{BE2} = 1V$

$\beta_1 = 75$ $\beta_2 = 15$

Solution

a. Vo_A = OP AMP output voltage
Io_A = OP AMP output current.

From Kirchoff's law,

$I_{E2} + I_{R5} - I_L - I_{R2} = 0$

Therefore, $I_{E2} = I_L + I_{R2} - I_{R5}$

Since Vo = 5V and $R_L = 1\Omega$, $I_L = 5A$
Therefore, $I_L = 5A$, $I_{E2} = (\beta_2 + 1) I\beta_2$

Therefore, $I\beta_2 = \left(\frac{I_{E2}}{\beta_2 + 1} \right)$

But $I_{E2} \simeq I_L$, therefore $I_{\beta 2} = \left(\frac{5}{15 + 1} \right)$ -= 312.5mA

$I_{E1} = I_{\beta 2} + I_{R5} = 312 + I_{R5}$
$I_{R5} = \left(\frac{V_{BE2}}{R_5} \right)$
$I_{E1} = 312.5mA$
$I_{\beta 1} = (\underline{I_{E1}}) = \underline{312.5mA} = 4.1mA$
$\beta_1 + 1 \qquad 76$
$V_{R4} = I_{\beta 1} R_4 = (4.1mA)(510) = 0.0041A\ (510) = 2.1V$

Therefore, the output voltage of the opamp is

$V_{OA} = 5V + V_{BE2} + V_{BE1} + V_{R4}$

$= 5V + 1 + 0.8 + 2.1 = 8.9V$

The output current of the opamp is the same as I_{B1},

$I_{OA} = I_{\beta 1} = 4.1mA$

b. For the circuit to work properly the opamp must be within the linear region and the Vi must be at least 2 Volts greater than V_{oA}. Therefore Vi ≥ 11V.

3.4 Protection Circuits

The performance of power transistors is affected by a number of factors such as Power dissipation capabilities, maximum voltage and current rating, maximum junction temperature; etc. This factor restricts the operation of the transistor to an area on the V & I curves known as the Safe Operating Area (SOA).

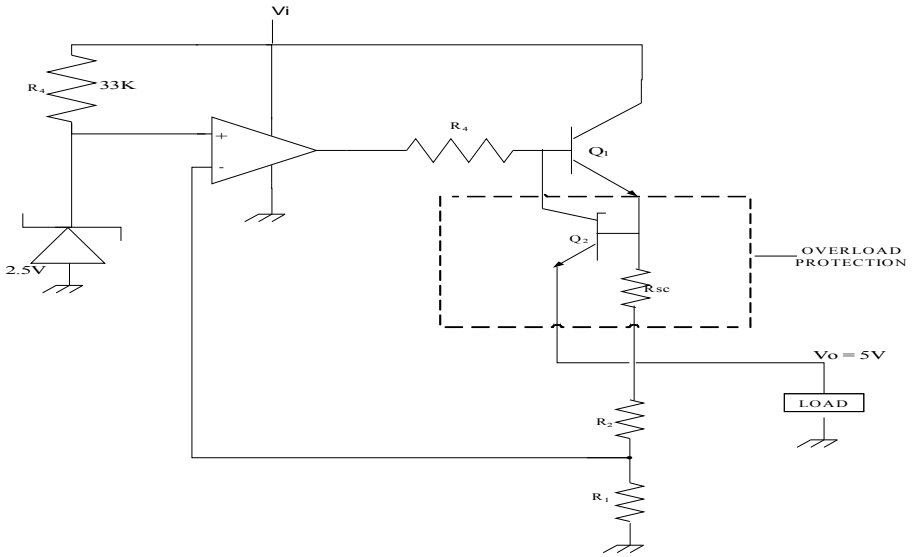
The SOA is defined as the area on the V and I curve within which the device can be operated without the risk of failure or degradation. To ensure reliable operation, regulators are equipped with additional circuits which serves to limit the current or switch off the transistors

should they be pushed outside the SOA. These circuits are inactive under normal operating conditions and get activated as soon as the SOA boundary is approached.

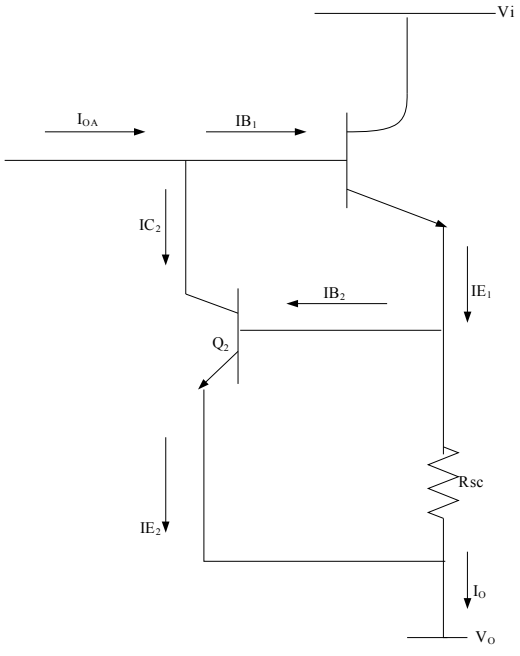
Examples of these circuits are:

1. Overload Protection

The purpose of this circuit is to prevent the current through the series pass transistor from exceeding a predetermined value. This is also known as short circuit protection.



The protection circuit alone is shown below

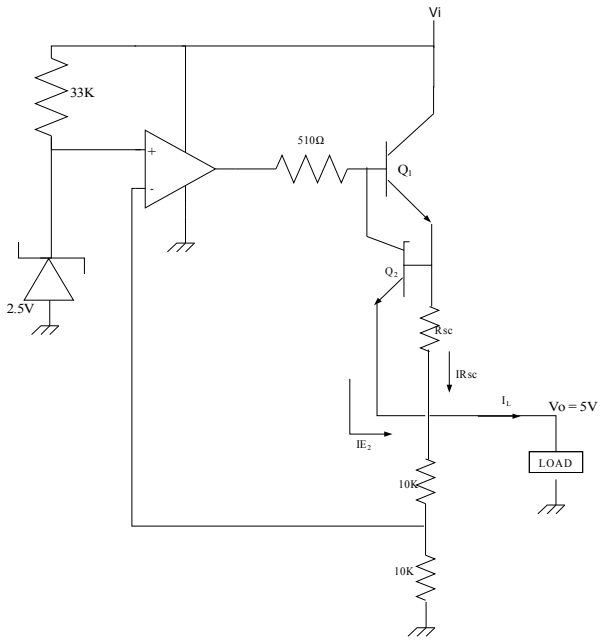


A single transistor Q_2 and R_{SC} is used to implement the circuit. The function of R_{SC} is to sense I_{E1} (Io) and develop a voltage drop of sufficient magnitude to switch on Q_2 when Io reaches the preset value.

$$R_{SC} = \left(\frac{V_{BE2(on)}}{I_{E1\max}} \right) = \frac{0.7}{I_{O\max}}$$

Under normal conditions, Io $\leq I_{E1max}$ and the voltage is insufficient to switch on Q_2.But when Io = I_{E1max} = I_{omax},the voltage across R_{SC} is such that Q_2 is turned on (V_{be} is attained). Then current in excess of I_{B1max} is diverted to Q_2 as I_{C2}.

Example



In the circuit above,

$\beta_i = 75$, $V_{BE1} = 0.8V$, $\beta_2 = 150$, $V_{BE2} = 0.7V$, $R_{SC} = 2.2\Omega$, $V_i = 12V$
For the overload protection,

$$R_{SC} = \frac{0.7}{I_{(RSC)}}$$

$$I_{RSC} = \frac{0.7}{2.2} = 0.318 = 0.32A$$

The maximum current as set by the overload protection is 320mA.

a. With $R_L = 25\Omega$, the actual load current becomes –
$I_L = \frac{V_L}{} = \frac{V_o}{} = \frac{5}{} = 0.2 = 200mA$. $I_{C1} = 200mA$, $I_{C2} = 0mA$

$R_L \quad R_L \quad 25$

$V_{RSC} = I_{LRSC} = 2.2 \times 0.2 = 0.44V.$

The voltage drop across $R_{SC} = 0.44V$ but a value of 0.7V is needed to switch Q_2 on. So with 0.44V,Q_2 is off and the protection circuit is in active.

b. With $R_L = 10\Omega$,

$$I_L = \frac{V_o}{R_L} = \frac{5}{10} = 0.5 = 500mA$$

$V_{RSC} = I_L R_{SC} = 0.5 \times 2.2 = 1.1V$

The voltage across $R_{SC} = 1.1V$ so the transistor Q_2 is switched on.

But $I_{L(max)} = 320mA$, therefore $V_{RL} = 0.32 * 10\Omega = 3.2V$. Vo = 3.2

$V_{B1} = V_{RL} + V_{BE1} + V_{BE2}$

$V_{B1} = 3.2 + 0.7 + 0.8 = 4.7V.$

But $V_n = \frac{V_o R_1}{R_1 + R_2} = \frac{3.2\ (10K)}{20K}$ Since $V_o = I_{Lmax} V_L = 3.2V$

$V_n = 1.6V$, $V_p = 2.5V$

Maximum output swing of the opamp is 2 volts less than V_i

Therefore $V_o = 12 - 2 = 10V.$

$$I_{(\text{output current of opamp})} = \frac{(VOA - V_{B1})}{R_4} = \frac{10 - 4.7}{510}$$

$I_{OA} = 10.4mA$

But $I_{B1} = \frac{I_{C1}}{\beta}$

Therefore $I_{B1(max)} = \beta I_{C1max}$, $I_{E1max} = I_{L(max)}$

$I_{B1(max)} = (75 + 1)$

$$I_{B1(max)} = \frac{I_{E1max}}{(\beta+1)} = \frac{320mA}{76} = 4.2mA$$

The balance of I_{OA} is absorbed by Q_2.

Therefore $I_{C2} = I_{OA} - I_{B1max} = 10.4 - 4.2$

$I_{C2} = 6.2mA$, $I_{B2} = \frac{I_{C2}}{\beta_2} = 0.04mA$

$I_{B2} + I_{C2} = I_{E2} \simeq 6.2mA$

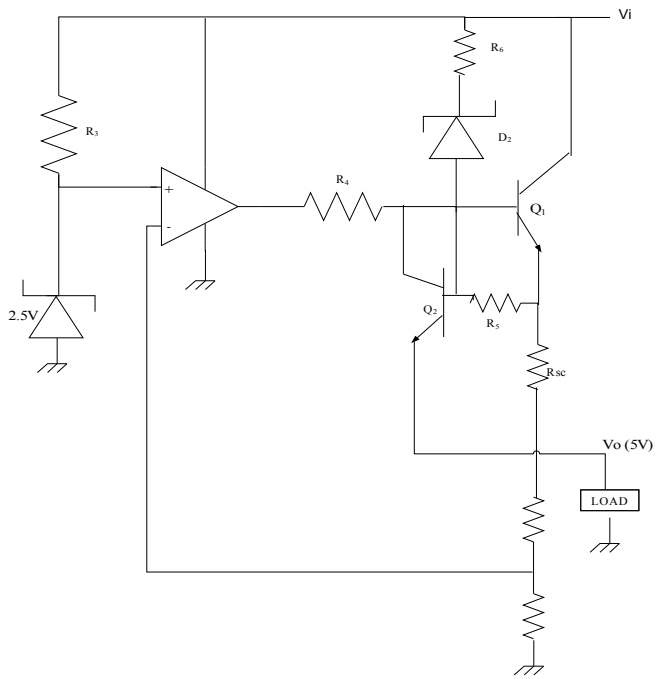
The final current delivered to the load is given by

$I_L = I_{RSC} + I_{E2}$ …….Kirchoff's current law.

$I_L = 320 + 6.2 = 326.2mA.$

2. SOA Protection

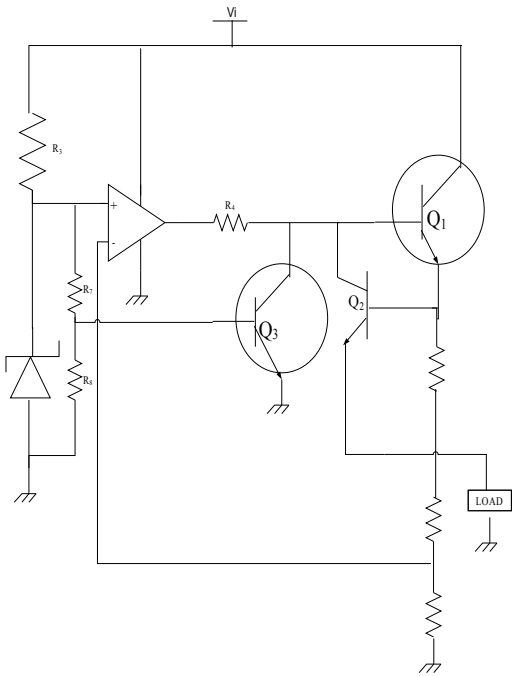
To restrict the BJT within the SOA,I_c must be reduced as V_{CE} rises above a safe level. This protection is used in circuits with a high possibility of transients or spikes in the unregulated input.



For values of V_i insufficient to turn on D_2 the protection remains inactive. From the zener diode characteristic curve below, when the voltage difference between V_i and V_o is beyond V_{Z2}, the zener diode begins to conduct. This forces Q_2 to also conduct because I_{Z2} will supply I_{B2} and when Q_2 begins to conduct, I_{B1} is reduced and the current output of the circuit is limited. This circuit is achieved by R_6, R_5, D_2. R_6 limits the current through D_2 and R_5 decouples Q_2 base from the Low Impedance point at Q_1's emitter.

3 Thermal Shut down

This form of protection which is mostly used in high power regulators due to possibility of damage due to self heating is implemented by sensing the elements junction temperature and reducing the power dissipation until the temperature drops to a tolerable level. The circuit is shown below:



As temperature increases, the value of V_{BE3} reduces to a value set by R_7 & R_8 and Q_3 starts conducting.The protection is achieved by using Q_3, R_7 and R_8.The basis for this operation is that V_{be} of a diode varies with temperature.

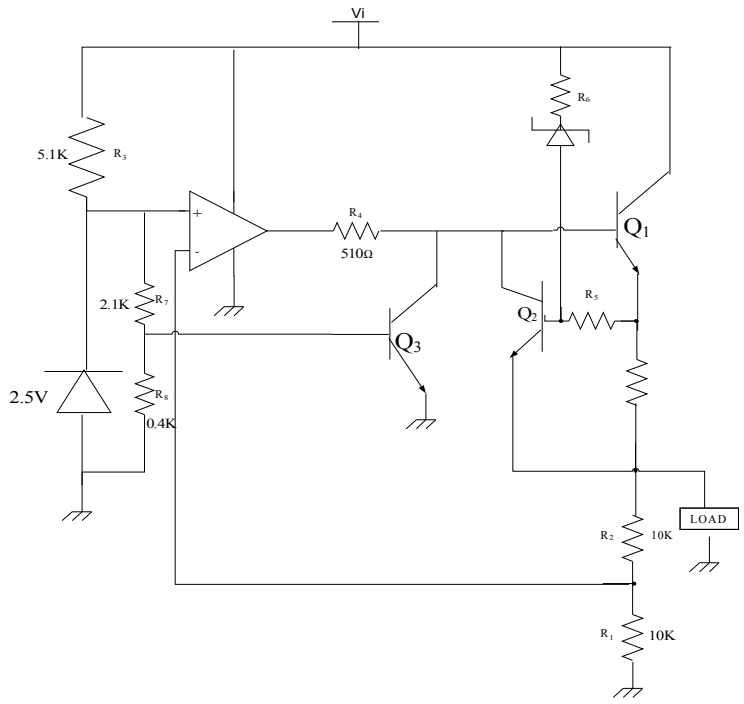
$$\frac{\delta V_{BE3}}{\delta T} = -2mV/^oC$$

At 25^{o}C, $V_{BE3} \simeq 700mV$.

As temperature increases to 175^{o}C, the value of V_{BE3} = 700mV – (175 – 25)(2)= 400mV.

This value is provided by the R_7 and R_8.When Q_3 is switched on, it reduces the I_{B1} which in turn reduces the output current. For fast response, Q_3 is usually glued to Q_1 to provide excellent thermal coupling.

The three forms of protection can be implemented in one circuit diagram as shown below



3.5 Integration Circuit Regulators

There are different types of IC voltage regulators. Some of these include:

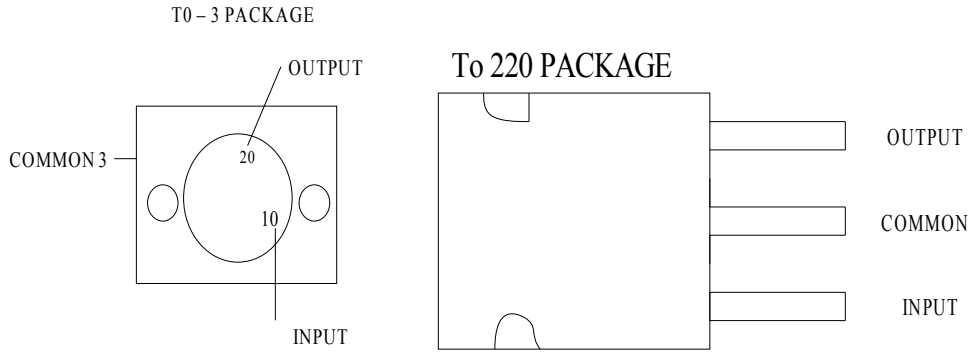
(1) Three terminal Fixed Voltage Regulators e.g. μa7800 series (+), μA7900 series (-)
(2) There terminal adjustable Regulators e.g. LM 317 (+), LM 337 (-)
(3) Four terminal adjustable Regulators μA78G
(4) Dual Tracking Regulators
(5) Low Dropout Voltage Regulators.

1. Three Terminal Fixed Voltage Regulators

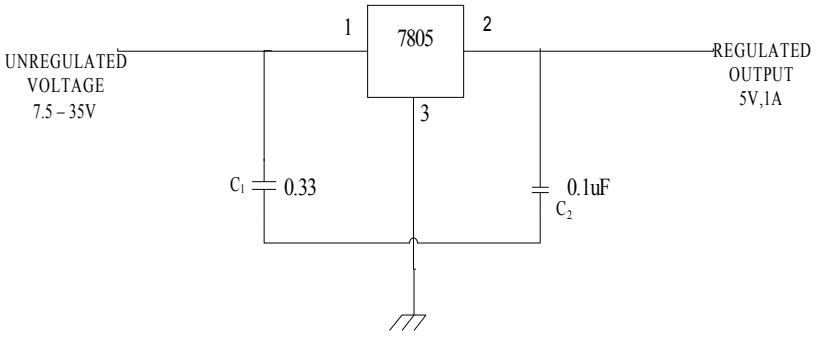
These regulators come with 3 pins, one each for unregulated input, regulated output and ground. They are produced to specific voltage values. Examples of these include the LM 78XX series for positive voltage and the LM 79XX for the negative voltage. The last two digits specify the output voltage of the chip.

LM 7805	LM 7905
LM 7806	LM 7906
LM 7812	LM 7912
LM 7815	LM 7915
LM 7824	LM 7924

The low power versions are available in plastic or metal packages like small transistors while high power versions are packaged in TO-3 type metal cans or TO 220 type moulded plastic packages.



The device will generate the specified output provided. The input is greater than the required output by 2.5V.This value is known as the drop out voltage and provided the output voltage is not exceeded.

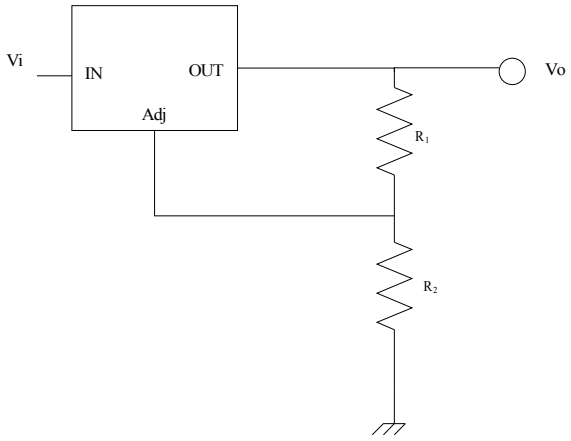


The data sheets recommend the use of two capacitors, C_1 which alters out the effect of stray inductance in the input wires and C_2 which improves the transient response to sudden load current changes.

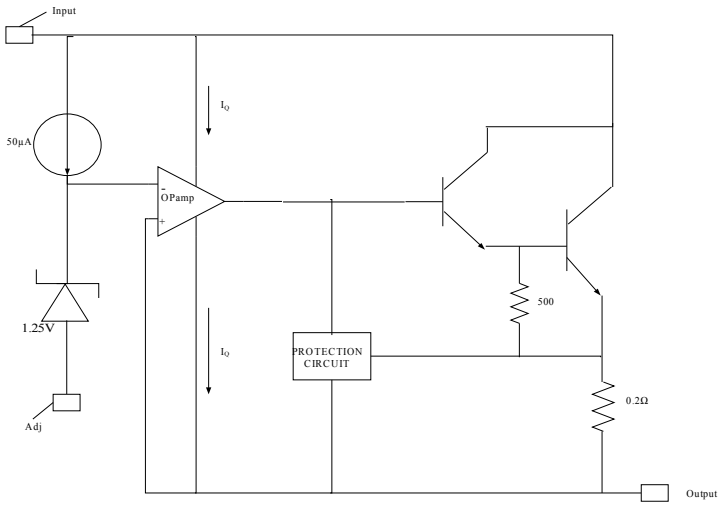
Other examples are the LM 340 (Positive regulator) and the LM 320 negative regulator; etc.

2 Three Terminal Adjustable Regulators

These types of regulators rely on external resistors to set the output voltage. Products in this category include the LM 317 (Positive) and the LM 337 (negative) regulators.



The common terminal is floated and now used as the adjustment pin.
The functional diagram of the LM 317 is shown below.



Once the circuit is powered, the error amp drives Vo to whatever value is needed to make Vn = Vp.

Therefore Vo = V_{ADJ} + 1.25V

The purpose of R1 and R2 is the setting of the value of Vo.

From a given formula (from data sheets)

Vo = (1 + $\frac{R_2}{R_1}$) (1+ $\frac{50\mu A}{1.25V/R_1}$) 1.25V

Current through R_1 is given to be 5mA.

Therefore, the equation above simplifies to

Vo = (1 + $\frac{R_2}{R_1}$) 1.25

By varying R_2 , Vo can be adjusted to any value in the range of $1.25 \leq Vo \leq 35V$.

The lower limits correspond to $R_2 = 0$, (i.e. Adj is grounded.)

11.0 CONCLUSION

In this unit you have been introduced to the basic principles of the DC power amplifier, its applications and the design procedure.

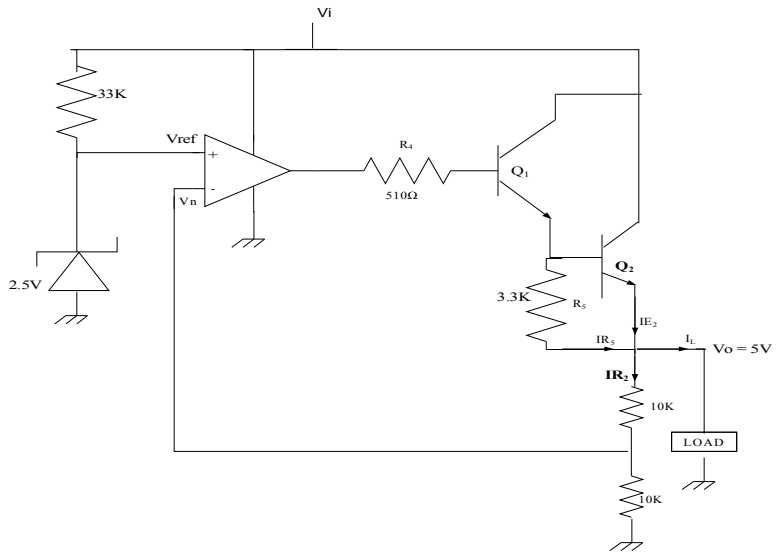
12.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of the Dc power supply and have been able to derive the different parameters of the DC power supply circuit.

13.0 TUTOR-MARKED ASSIGNMENT

From the circuit below:

(1) Determine the voltage and current at the OP AMP output
(2) Find the minimum value of Vi at which the circuit will still function properly.



RL = 2Ω

$V_{BE1} = 0.8$ $V_{BE2} = 1V$

$\beta_1 = 75$ $\beta_2 = 15$

14.0 REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

UNIT 3 HEAT SINKS

CONTENTS

1.0 INTRODUCTION

A heat sink is a metallic material attached to an integrated circuit chip or a high power dissipating transistor. Its aim is to increase the total surface area of the component thereby increasing the rate of heat dissipation of the component .Its purpose is to ultimately prolong the life of the component.

2.0OBJECTIVES

At the end of this unit, student should be able to:

- identify heat sinks
- analyze the Heat sink design
- design heat sinks for amplifier circuits.

3.0 MAIN CONTENT

3.1 Heat Sinks

The heat dissipated in Integrated circuits and other electronic circuits must be removed or the circuits will be damaged due to excessive temperature rise. Devices based on P-N junction like transistors, diodes, Integrated circuits are the most affected as all the heat is produced at the P-N junction. The power dissipated in the transistor increases its temperature above the ambient temperature. If the device or junction temperature T_j becomes too high, the transistor may suffer permanent damage.

The maximum allowable chip temperature referred to as the maximum junction temperature is given in data sheets. For silicon devices, this is usually in the range of 150^0C TO 200^0C.

To prevent excessive junction temperature build up, heat must be expelled from the silicon chip to the surrounding package structure and then to the ambient. Heat transfer is directly proportional to surface area so the larger the surface area of the chip, the faster the heat transfer from the chip. But design specifications place limits on the chip area, so an approach at increasing the surface area of chips is through the use of heat sinks.

A heat sink is a metal structure usually with fins that is bonded, clipped or clamped to the device package to facilitate heat flow from case to ambient.

3.2 Thermal Resistance

As the chip's temperature increase with respect to the ambient, at thermal equilibrium this increase is proportional to the internally dissipated power.

$T_J - T_A \simeq \theta_{JA} P_D$.

where T_J and T_A are junction and ambient temperatures respectively.
P_D is the dissipated power and
θ_{JA} is the junction to ambient thermal resistance in ^{o}C/W.

The rate of loss of heat is proportional to the temperature difference between the junction and the ambient (case).

$$\theta = \frac{\Delta T}{P} = \frac{TJ - TA}{P}$$

The thermal resistance and maximum allowable junction temperature set an upper limit on the power dissipation capabilities of devices such as power amplifiers, voltage regulators e.t.c no heat sink is used, the device will be said to be operating in free air.

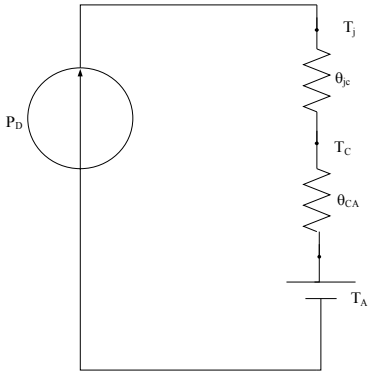
3.3 Free Air Operation

In free air operation, the thermal resistance consists of two components,
$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = thermal resistance from junction to case

θ_{CA} = thermal resistance from core to ambient

This can be illustrated in the diagram below:



The values for θ_{JC} and θ_{JA} are usually provided but θ_{CA} must be calculated.

3.4Heat Sink Operation

When a heat sink is used, the equation gets modified

$T_J - T_A = P_D\theta_{JA}$
Where $\theta_{JA} = (\theta_{JC} + \theta_{CS} + \theta_{SA})$

θ_{JC} = thermal resistance between junction and case

θ_{CS} = thermal resistance between case and heat sink

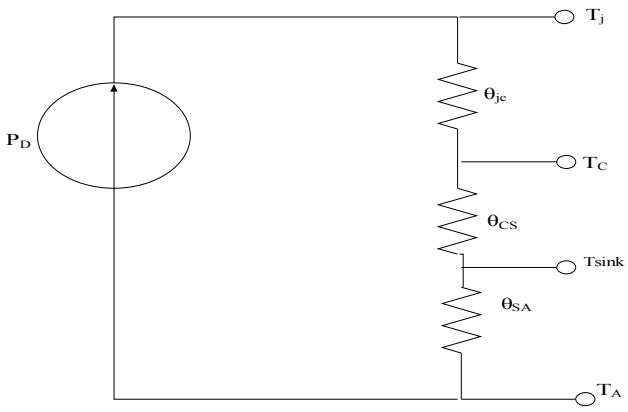
θ_{SA} = thermal resistance between heat sink and ambient.

Therefore, $T_J - T_A = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA})$

Where P_D = Power dissipated in the device.
The presence of the heat sink alters the thermal resistance between case and ambient.

$\theta_{CA} = \theta_{CS} + \theta_{SA}$

The Electrical diagram for this is shown below



Example 1

Determine the maximum power dissipation in a MOSFET with the following parameters:

$\theta_{JC} = 1.75^OC/ W$, $\theta_{CS} = 1^OC/ W$, $\theta_{SA} = 5^OC/ W$, $\theta_{CA} = 50^OC/ W$, $T_A = 30^OC$ and $T_{jmax} = 150^OC$.

Without Heat Sink

$T_J - T_A = P_D (\theta_{JC} + \theta_{CA})$
$150 - 30 = P_D (1.75 + 50)$
Therefore, $P_D = \frac{120}{51.75} = 2.32W$

With Heat Sink

$T_J - T_A = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) = 150\text{-}130 = P_D (175+1+5)$
$P_D = \frac{150-30}{(1.75+1+5)} = \frac{120}{7.75} = 15.5W$

From the example, the heat sink allows power to be dissipated in the device while keeping the temperature below T_J.

Example 2

A given transistor has $\theta_{JA} = 200^OC/ W$, $T_A = 30^OC$.

Power dissipation of 100mW will give a T_j of $P_D = 100mW = 0.1W$

$\Delta T_j = P_D\theta_{JA} = 200 * 0.1 = 20^OC$.

The new junction temperature $T_j = T_A + \Delta T_j$

Therefore $T_j = 30^oC + 20^oC = 50^oC$.

The thermal contact between the case and the heat sink must be of low thermal resistance and a thermally conducting paste should be used to bond the heat sink to the case.

Heat sinks are made in many shapes and sizes. They are often painted in black to aid radiative heat transfer. Cooling fans are also used if the heat sink gets too hot, this is called forced convection. Fans improve the dissipation of a heat sink by a factor of two or three and this leads to smaller heat sink design. Aluminium due to its light weight and low resistivity is often used in heat sink construction.

4.0 CONCLUSION

In this unit you have been introduced to the basic principles of the Heat sinks, its applications and the design procedure.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of the heat sink and have been able to derive the design procedure for each application of the heat sink.

6.0 TUTOR-MARKED ASSIGNMENT

(1) 5V regulator is to satisfy the following requirements:

$0^oC \leq T_A \leq 60^OC$, $I_{O(max)} = 0.8A$, $V_{i(max)} = 12V$, $T_{Jmax} = 125^OC$.

Select a suitable heat sink for it.

(2) A silicon transistor has $\theta_{JC} = 10^OC/W$ and $\theta_{CA} = 30^OC/W$.

(a) Determine P_{DMAX} of $T_A = 30^OC$ and $T_J = 150^OC$.
(b) When a heat sink of $\theta_{HA} = 7^OC/W$ is used, determine the T_J of $P_D = 5W$

7.0 REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

MODULE 4

Unit 1 Boolean Algebra
Unit 2 Logic Gates
Unit 3 Karnaugh Map

UNIT 1 BOOLEAN ALGEBRA

CONTENTS

1.0 INTRODUCTION

The objective of this course is to introduce the student to the field of digital systems. Starting at the fundamental level of Boolean algebra and the different laws used in the resolution of digital electronics circuits.

2.0 OBJECTIVES

At the end of this unit, students should be able to:

- the understanding of Boolean algebra and its laws
- the introduction of the Boolean algebraic identities
- the introduction of the De Morgan's theorem.

3.0 MAIN CONTENT

3.1 Boolean Algebra

Boolean algebra is the basic mathematics for the study of logic design .Basic laws of Boolean algebra are implemented as switching devices called logic gates. A Boolean variable can take on two values '0' and '1', 'T', 'F or H,L or ON,OFF . Boolean operations transform Boolean Variables the basic operations are NOT, AND, OR

More complicated Boolean Functions can be derived from the basic Boolean operations.

Basic Boolean algebraic identities

A + 0 = A
A + 1 = 1
A + A = A
A + A = 1
0*A = 0
1*A = A
A*A = A
A*A = 0
$\overline{\overline{A}} = A$

Laws of Boolean algebra

Commutative Law

(a) $A + B = B + A$
(b) $A\,B = B\,A$

Associate Law

(a) $(A + B) + C = A + (B + C)$
(b) $(A\,B)\,C = A\,(B\,C)$

Distributive Law

(a) $A\,(B + C) = A\,B + A\,C$
(b) $A + (B\,C) = (A + B)\,(A + C)$

Identity Law

(a) $A + A = A$
(b) $A\,A = A$

Redundance Law

(a) $A + A\,B = A$
(b) $A\,(A + B) = A$

Other Boolean Identities

(a) $A\bar{B} + AB = A$
(b) $(A+B)(A+\bar{B}) = A$

(c) $\overline{A} + A = 1$

(d) $\overline{A}\ A = 0$

(e) $A + \overline{A}\ B = A + B$

(f) $A\ (\overline{A} + B) = A\ B$

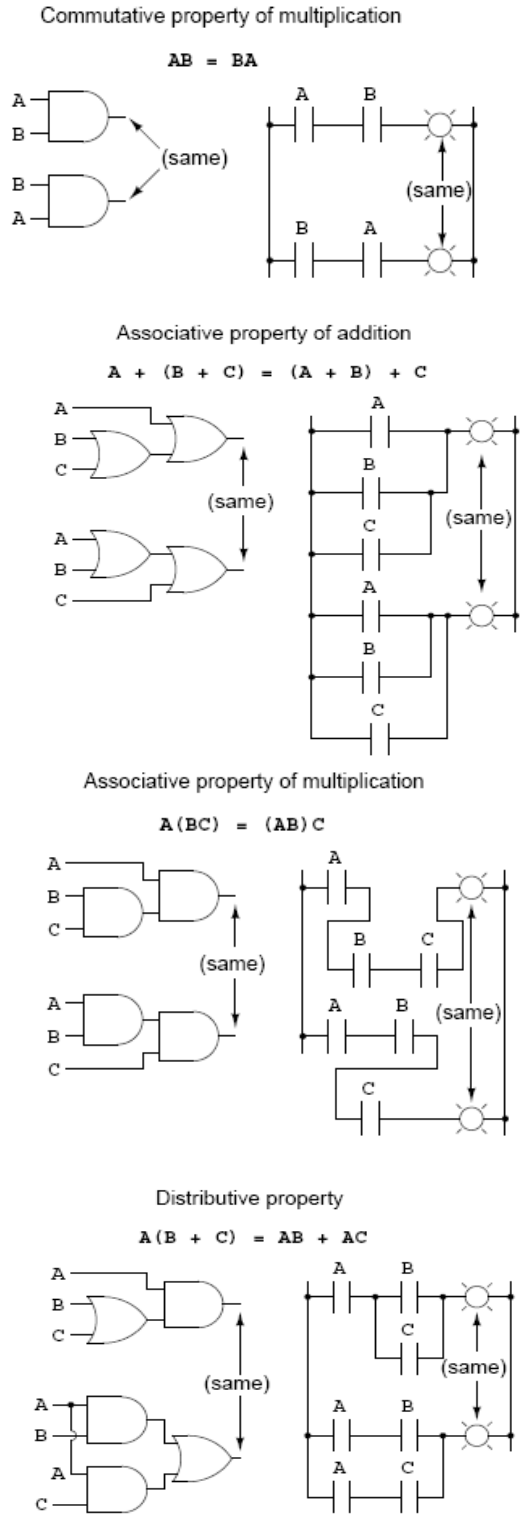


Fig 9.1 Boolean algebraic identities

Example 1

Prove (a) $A + \overline{A}B = A + B$

Solution

(1) Algebraically:

$$A + \overline{A}B = A1 + \overline{A}B$$
$$= A(1 + B) + \overline{A}B$$
$$= A + AB + \overline{A}B$$
$$= A + B(A + \overline{A})$$
$$= A + B$$

(2) Using the truth table:

Table 9.1: Truth table for the example 9.1

A	B	A+B	$\overline{A}B$	A+$\overline{A}B$
0	0	0	0	0
0	1	1	1	1
1	0	1	0	1
1	1	1	0	1

3.2 DeMorgan's Theorem

DeMorgan's Theorem allows gates to be converted to others by simply inverting the inputs of the selected gate. More specifically, you can convert gates to others if the following steps are followed accordingly:

1. Complement all inputs.
2. Convert all AND operations to ORs
3. Convert all OR operations to ANDs
4. Complement the entire expression.

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$
$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

The key to the theorem is break the line, change the sign

The truth table to prove the theorem is shown below.

A	B	$\overline{A}$	$\overline{B}$	$\overline{A + B}$	$\overline{A} \cdot \overline{B}$	$\overline{A \cdot B}$	$\overline{A} + \overline{B}$
0	0	1	1	1	1	1	1
0	1	1	0	0	0	1	1
1	0	0	1	0	0	1	1
1	1	0	0	0	0	0	0

4.0 CONCLUSION

In this unit you have been introduced to the basic principles of the Boolean algebra and the demorgans theorem.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of Boolean algebra, the De Morgan's theorem and the different rule that govern the use of Boolean algebra in digital electronics.

6.0 TUTOR-MARKED ASSIGNMENT

(1) Simplify the expression using Boolean algebra

$\overline{x}\,\overline{y} + xy + \overline{x}y$

$\overline{x} + xy + x\overline{z} + x\overline{y}\,\overline{z}$

$[A\overline{B}(C + BD) + \overline{A}\,\overline{B}]C$

$\overline{A}BC + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}\,C + ABC$

(2) Apply DeMorgan's theorems to the following expression $\overline{\overline{A + B\overline{C}} + D(\overline{E + \overline{F}})}$.

7.0 REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

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UNIT 2 LOGIC GATES

CONTENTS

15.0 INTRODUCTION

A logic gate is an electronic circuit which makes logic decisions. It has one output and one or more inputs. They are the fundamental blocks with which digital systems are built. The output is a result of the implementation of the logical algebra known as the Boolean algebra.

16.0 OBJECTIVES

At the end of this unit, student should be able to:

- identify the different logic gates
- analyze circuits with logic gates
- generate other gates from the universal gates.

17.0 MAIN CONTENT

3.1 Logic Gate

One characteristic of this Boolean algebra is that the variables can only assume one of the two values 0 and 1. Where 0 (zero) can represent off, low, minus or false depending on the convention used while 1 (one) takes the opposite state. The gates are available in various IC families, popular among them are the transistor- transistor logic (TTL), emitter coupled logic (ECL), metal oxide semiconductor (MOS) and the complementary metal oxide semiconductor (CMOS). Most of these

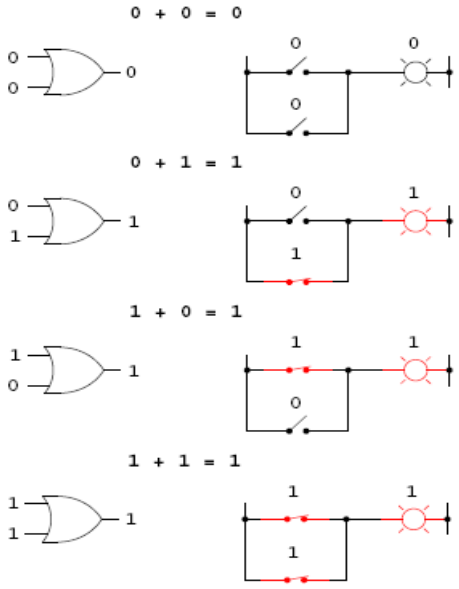
families have their unique characteristics and qualities for example, the TTL families consume considerable quiescent current while the CMOS which is factor than the TTL consumes zero quiescent current (though it is more delicate) among other properties.

We shall be considering the following gates and their truth table OR gate, AND gate, NOT gate, NOR and NAND gates. Another gate we will look at is the exclusive OR gate. The logic used to determine the state of the variables can either be positive or negative. In the positive logic, where there are two voltage values, the more positive of the voltage represents the high while if we are operating on the negative logic, the more negative value would represent the high state.

3.2 OR Gate

The OR gate is a gate which produces a high output of any or both (all) if its inputs are high. It symbolizes logic addition.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1



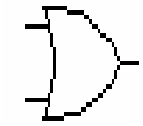


Figure 2 input OR gate

From the diagram (b) we see that so long as any of the switches is closed the bulb will light up. The OR gate represents the Boolean equation;

$A + B = C$

NOTE: a truth table is a table which gives the output state for all the possible input combination.

This OR gate can also be known as an inclusive OR gate because it includes the case when both input are true. Gates can have any number of inputs but standard packages contain four 2- input gates, three 3-input gates. The OR gate can also be derived from discrete circuits. e.g. diodes and transistors.

3.3 AND Gate

The AND gate is a logic gate which will give a high output if and only if all its inputs are high. It symbolizes logical multiplication.

SYMBOL

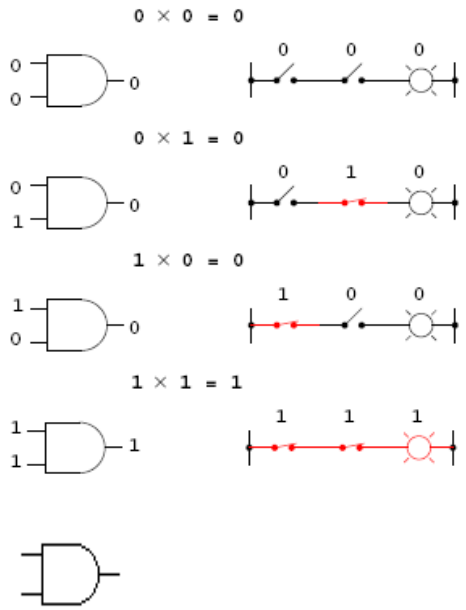


Figure 2 –input AND gate

The AND gate works on the Boolean algebra

$$A \times B = C$$

From the diagram it can be seen that an AND gate can be represented by a series circuit. For the lamp to come on, the switches A and B must be on. Below are truth tables for two and three input AND gates.

Two input AND gate. C = output

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Three input AND gate. D = output

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0

The AND gate can also be realized using the diode and the transistor.

3.6 The NOT Gate (Inverse)

The NOT gate is also known as an inverter because it inverts the input signal. It has one input and one output terminal. The logical symbol for negation or inversion is a bar over whose function is to indicate the opposite state. The symbol of the NOT gate is shown below. Truth table for the NOT gate

A	B
0	1
1	0

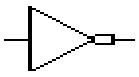


Figure NOT gate symbol

$B = \overline{A}$

NAND/NOR GATES

The gates (AND/OR) discussed above can be combined with the NOT gate to produce other gates known as the NOR and the NAND gates. This is achieved by inverting the inputs of the gates.

3.7 The NOR Gate

The NOR gate is a combination of the NOT and the OR gate. The NOT gate function is a reverse of the OR gate function so it will have an output of 1 only when all its inputs are 0. The output of the NOR gate is fed to the input of the NOT gate to give NOR.

The NOR gate is also referred to as a universal gate because it can be used to simulate OR, AND and NOT gate functions. The NOR gate

symbol is an OR gate symbol with a bubble at the output pin as shown below.

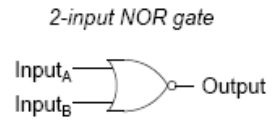
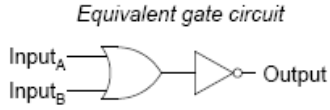


Figure 2-input NOR gate

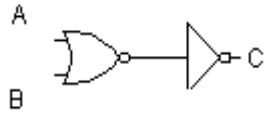


Truth table for the 2 input NOR gate

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

OR GATE FUNCTION

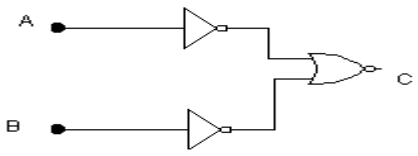
By placing another inverter at the output of the NOR gate the output is re-inverted giving an OR gate function.
OPERATION



$A + B = \overline{A + B} = C$

AND GATE FUNCTION

In this case, two inverters are used in the input. The inputs are inverted before going into the NOR gate and thus the output of the NOR gate is:



$C = A + B$

NOT GATE FUNCTION

In this case the two inputs are tired together and the output is A + A which by demorgan is A. the OR and AND gates can also be derived from using purely NOR gates.

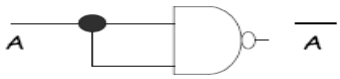
3.8 NAND Gate

In this case the circuit of the AND gate is fed to the input of an inverter. The gate gives an output of 1 if either A or B or both are 0. The NAND gate is also a universal gate as it can be construed as shown to get either an AND gate or an OR gate operation. The NAND gate symbol is an AND gate symbol with a bubble at the output pin as shown below.

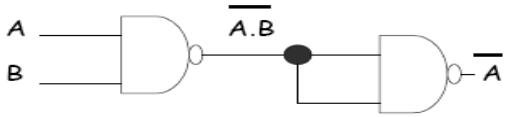
$C = A.B$

A	B	C
0	0	1
0	1	0
1	0	1
1	1	0

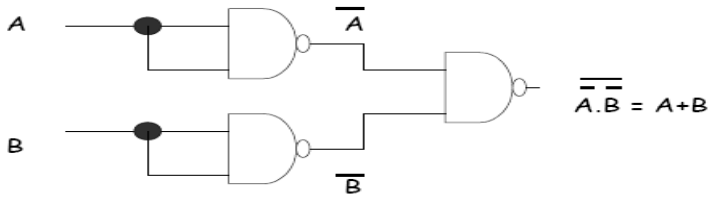
Implementation of a NOT gate using a NAND



Implementation of an AND gate using a NAND

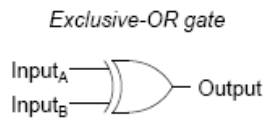


Implementation of an OR gate using a NAND



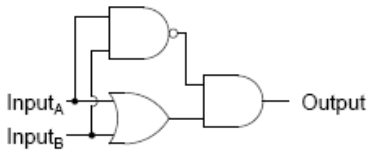
3.9 XOR Gate

Exclusive-OR gates output a high, (1) logic level if the inputs are at *different* logic levels, either 0 and 1 or 1 and 0. Conversely, they output a low (0) logic level if the inputs are at the *same* logic levels. The Exclusive-OR (sometimes called XOR) gate has both a symbol and a truth table pattern shown below:



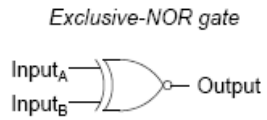
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

There are equivalent circuits for an Exclusive-OR gate made up of AND, OR, and NOT gates, just as there were for NAND and NOR gates. A rather direct approach to simulating an Exclusive-OR gate is to start with a regular OR gate, then add additional gates to inhibit the output from going, high, (1) when both inputs are high. (1):



3.10 XNOR Gate

Exclusive-NOR gate, otherwise known as the XNOR is equivalent to an Exclusive-OR gate but it has an inverted output. The truth table for this gate is exactly opposite as for the Exclusive-OR gate:



A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

Example 1

A digital signal 101011 is applied to a NOT gate what will be the NOT gate output.

Input = 1 0 1 0 1 1

Output = 0 1 0 1 0 0

SELF ASSESSMENT EXERCISE

1. Two signals A = 1 0 1 1 0 1 and B = 1 1 0 1 0 1 are fed to a 2 input AND gate sketch the output signal.

2. Convert the following Boolean expression to logic using different logic gates.
(A. B + C)

18.0 CONCLUSION

In this unit you have been introduced to the different logic gates, their symbols and applications.

19.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of the different types of logic gates.

20.0 TUTOR-MARKED ASSIGNMENT

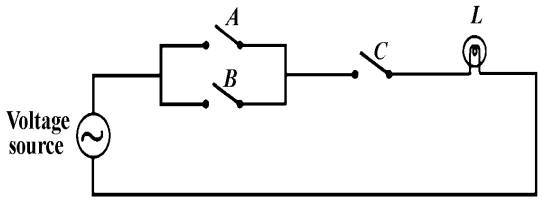
1) Two signals A = 1 0 1 1 0 1 and B = 1 1 0 1 0 1 are fed to a 2 input AND gate sketch the output signal.

2) Using DeMorgan's theorem, convert the following Boolean expressions to equivalent expressions that (i) have only OR and complement operations, and show that the functions can be implemented with NOR gates only; (ii) have only AND and complement operations, and show that the functions can be implemented with NAND gates only.

(a) $f = \bar{x}\,\bar{y} + \bar{x}z + \bar{y}z$

(b) $f = (y + \bar{z})(x + y)(\bar{y} + z)$

3) Express the switching circuit shown in the figure in binary logic notation and generate the truth table



21.0 REFERENCES/FURTHER READINGS

Fitchen F.C; (1972). *Transistor Circuit Analysis and Design*. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.

UNIT 3 KARNAUGH MAP

CONTENTS

1.0 INTRODUCTION

In the design of logic functions by means of logic gates, more than one solution is usually available for the implementation of a given logic expression and some combinations of gates can implement a given function more efficiently than others. The challenge in logic design is the assurance of having chosen the most efficient realization.

A very popular and easy to use procedure for simplifying logic design exists and it utilizes a map, describing all possible combinations of the variables present in the logic function of interest. This map is called a **Karnaugh map,** after its inventor. The karnaugh map consists of row and column assignments for two or more variables arranged so that all adjacent terms change by only one bit. Each map consists of 2^N **cells,** where N is the number of logic variables. Karnaugh maps allow us to convert a truth table to a simplified Boolean expression without using Boolean Algebra.

4.0OBJECTIVES

At the end of this unit, student should be able to:

- the understanding of the use of karnaugh maps in logic design
- the understanding of the use of karnaugh maps in simplification of logic design
- the understanding of conversion of truth tables to Boolean algebra
- the generation of digital logic circuits from truth tables.

3.0 MAIN CONTENT

3.1 Introduction to Karnaugh Maps

Karnaugh maps are a graphical way of simplifying a Boolean expression and thus simplifying the resulting circuit. A Karnaugh map is a completely mechanical method of performing this simplification, and so has an advantage over manipulation of expressions using Boolean algebra. Karnaugh maps are effective for expressions of up to about six variables. For more complex expressions the more advanced Quine-McKluskey method may be appropriate.

The Karnaugh map uses a rectangle divided into rows and columns in such a way that any product term in the expression to be simplified can be represented as the intersection of a row and a column. The rows and columns are labeled with each term in the expression and its complement. The labels must be arranged so that each horizontal or vertical move changes the state of one and only one variable. The figure 9.1 below shows karnaugh map with 2,3and 4 variables

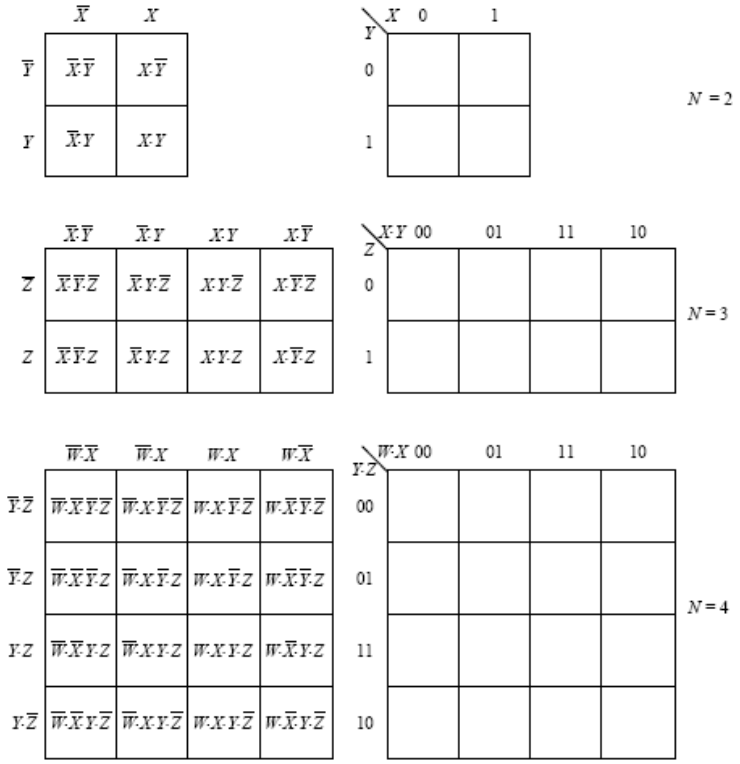


Figure 9.1 Karnaugh maps with 2, 3, 4 variables

3.2 Circuit Simplification Using Karnaugh Maps

The following steps are required to use a Karnaugh map to simplify an expression:

1. Draw a "map" with one box for each possible product term in the expression.
   The boxes must be arranged so that a one-box movement either horizontal or vertical changes one and only one variable. See Figure 9.1.
2. For each product term in the expression to be simplified, place a checkmark (or a 1) in the box whose labels are the product's variables and their complements.
3. Draw loops around adjacent pairs of checkmarks. Blocks are "adjacent" horizontally and vertically only, not diagonally. A block may be "in" more than one loop, and a single loop may span multiple rows, multiple columns, or both, so long as the number of checkmarks enclosed is a power of two.
4. For each loop, write an unduplicated list of the terms which appear; *i.e.* no matter how many times A appears, write down only one A.
5. If a term and its complement both appear in the list, *e.g.* both A and $\overline{A}$, delete both from the list.
6. For each list, write the Boolean product of the remaining terms.
7. Write the Boolean sum of the products from Step 5; this is the simplified expression.

Example 1

Simplify the Boolean expression below using karnaugh maps AB+ A$\overline{B}$.

Solution

This is an expression of two variables. A rectangle is drawn and divided so that there is a row or column for each variable and its complement.
Next, we place checks in the boxes that represent each of the product terms of the expression.

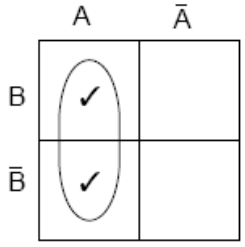


Figure 9.2: Karnaugh map for example 1

The first product term is AB, so a check is placed in the upper left block of the diagram, the conjunction of A and B.

The second is A$\overline{B}$, so we place a check in the lower left block. Finally, we draw a loop around adjacent pairs of checks. The loop contains A, B, A, and $\overline{B}$. We remove one A so that the list is unduplicated. The B and $\overline{B}$ "cancel," leaving only A, which is the expected result: AB+ AB = A.

Example 2

Simplify A$\overline{B}$ + $\overline{A}$B + $\overline{A}\overline{B}$ using K-Maps

Solution

There are two variables, so the K-Map is the same as in Example 1.
The solution will be derived using the following steps:
Place a check in the A$\overline{B}$ area.
Place a check in the $\overline{A}$B area.
Place a check in the $\overline{A}\overline{B}$ area.

Draw loops around pairs of adjacent checks.

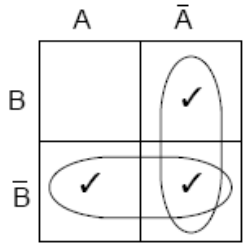


Figure 9.3: Karnaugh map for example 2

The Vertical loop contains $\overline{A}$, B, $\overline{A},\overline{B}$. Since $\overline{A}$ is duplicated, one of it is removed. B and its complement $\overline{B}$ both cancel out leaving only $\overline{A}$.

From the horizontal loop we have A, $\overline{B}$, $\overline{A},\overline{B}$.The duplicate $\overline{B}$ is removed and the A cancels out with its complement.
The Boolean sum of the manipulation is now $\overline{A}$+ $\overline{B}$ which is the answer.

3.3 Simplifying Logic Circuits Using Karnaugh Maps

The major advantage of Karnaugh maps is its ability to simplify logic design by simplifying the Boolean expression and/or truth table and eliminating unnecessary logic gates in a digital logic design.

Example 3

Given the truth table for a 3 input logic design:

(1) Generate the Boolean equation and sketch the logic circuit required to implement the truth table
(2) Simplify the logic design using K-maps and sketch the resultant logic circuit.

The output is the X column.

Table 9.2 Output of the 3 input logic circuit

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Solution

(1) From the truth table, the circuit generates an output when X = 1.The product of the terms at which X = 1 is taken out and summed together. This sum is known as sum of products and it is the Boolean expression that generates the truth table.

Products terms are: $\overline{A}\overline{B}\overline{C}$, $\overline{A}BC$ and ABC

Sum of products = $\overline{A}\overline{B}\overline{C} + \overline{A}BC + ABC$

The digital logic circuit based on the Boolean equation is given below. Note, the inputs are A, B and C and the complements are $\overline{A}\overline{B}\overline{C}$ The complements are generated by the use of inverters or NOT gates. ABC complements are fed into a 3 input AND gate while $\overline{A}BC$ is fed into another 3 input AND gate and ABC is fed into the third 3 input AND gate. The inputs of the three 3-input AND gates are fed together into a 3-input OR gate. The circuit diagram is shown below.

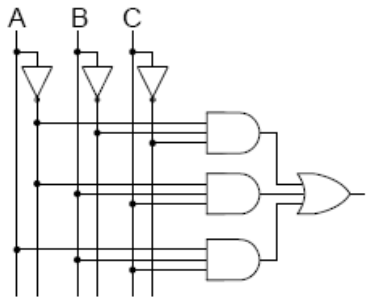


Figure 9.4: Digital logic circuit for example 3

(2) The truth table generates an expression with three product terms. A measure of the complexity of a digital logic circuit is the number of gate inputs. The circuit in

Figure 9.4 has 15 gate inputs. The Karnaugh map for the sum of products expression is shown in Figure 9.5 below.

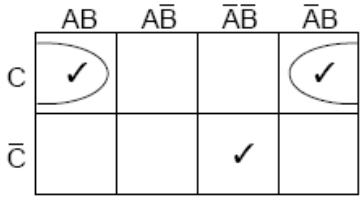


Figure 9.5 Karnaugh map for example 3

In this Karnaugh map, the large loop surrounds A B C and $\overline{A}BC$.It "wraps around" from the left edge of the map to the right edge. The A and $\overline{A}$ cancel, so these two terms simplify to BC. $\overline{A}\overline{B}\overline{C}$ is in a cell all by itself, and so contributes all three of its terms to the final expression.

The simplified expression is B C + $\overline{A}\overline{B}\overline{C}$ and the simplified circuit is shown in Figure 9.6. In the simplified circuit, one three-input AND gate was removed, a remaining AND gate was changed to two inputs, and the OR gate was changed to two inputs, resulting in a circuit with ten gate inputs.

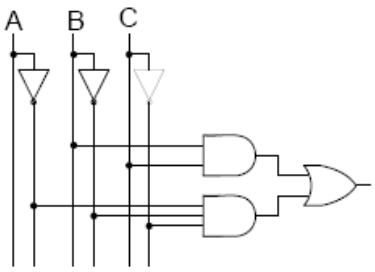


Figure 9.6: Simplified Circuit in example 3

4.0 CONCLUSION

In this unit you have been introduced to the use of the karnaugh map in simplification of digital logic circuits. The following observations are to be noted in the generation of loops in the K-maps. For maximum simplification, the loops are to be made as big as possible with big loops being the preferred size. The restriction is that the loop must be rectangular and enclose a number of checkmarks that is a power of two. When a map is more than two rows deep, *i.e.* when it represents more than three variables, the top and bottom edges can be considered to be adjacent in the same way that the right and left edges are adjacent in the two-by-four maps above. If all checkmarks in a loop are enclosed within other loops as well, that loop can be ignored because all its terms are accounted for.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of the Karnaugh Maps.

6.0 TUTOR-MARKED ASSIGNMENT

1 Given the following Karnaugh maps, determine their logic equation.

WX / Y	00	01	11	10
0	1	1	0	0
1	1	1	0	0

WX / Y	00	01	11	10
0	1	0	0	1
1	0	0	0	0

2) Given the truth table for a 3 input logic design,

(a) Generate the Boolean equation and sketch the logic circuit required to implement the truth table in Table 9.3

(b) Simplify the logic design using K-maps and sketch the resultant logic circuit.

The output is the X column.

Table 9.3 Output of the 3 input logic circuit

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3 Use a Karnaugh map to simplify A B C + A $\overline{B}\overline{C}$ + $\overline{A}\overline{B}\overline{C}$.

7.0 REFERENCES/FURTHER READINGS

Mendelson, Elliott, (1970). *Schaum's Outline of Theory and Problems of Boolean Algebra.* McGraw- Hill

Maddock R.J and Calcutt D.M (1994). *Electronics*: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). *Electronics Circuit Analysis and Design*. McGraw-Hill Publishers.